

Compal Confidential

PAGANI M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point

Date : 2011/11/22
Version 0.1

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address


Device	Address
PCH (Reserve)	1010 0110b


SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH				V	V					V
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	CR+ Giga LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

SATA	DESTINATION
SATA0	HDD,JHDD1
SATA1	m-SATA,JMINI2
SATA2	ODD, JODD1
SATA3	None
SATA4	None
SATA5	None

Option	@	CONN@	PX@	
UMA	X	X	X	
DIS	X	X	V	

USB Port Table

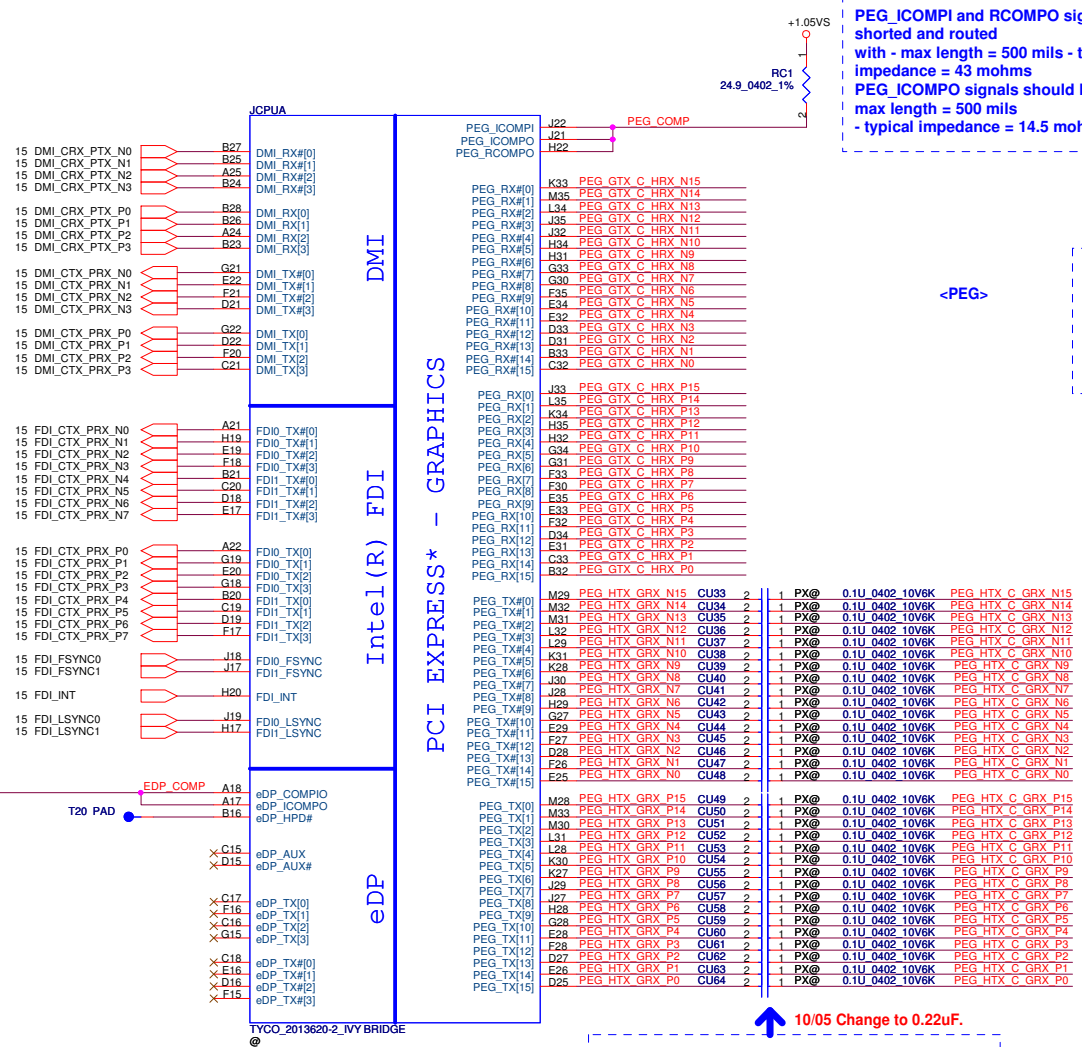
USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB3.0
		1	USB3.0
	UHCI1	2	USB3.0
		3	USB2.0 FRP
	UHCI2	4	X
		5	m-SATA
EHCI2	UHCI3	6	X
		7	X
	UHCI4	8	Camera
		9	USB2.0 and sleep charger
	UHCI5	10	minPCIE-WLAN/BT
		11	X
	UHCI6	12	X
		13	X

USB 3.0	Port	3 External USB Port
	0	USB3.0
	1	USB3.0
	2	USB3.0(SB)

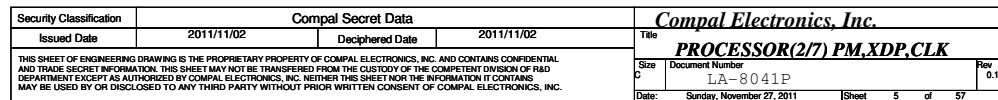
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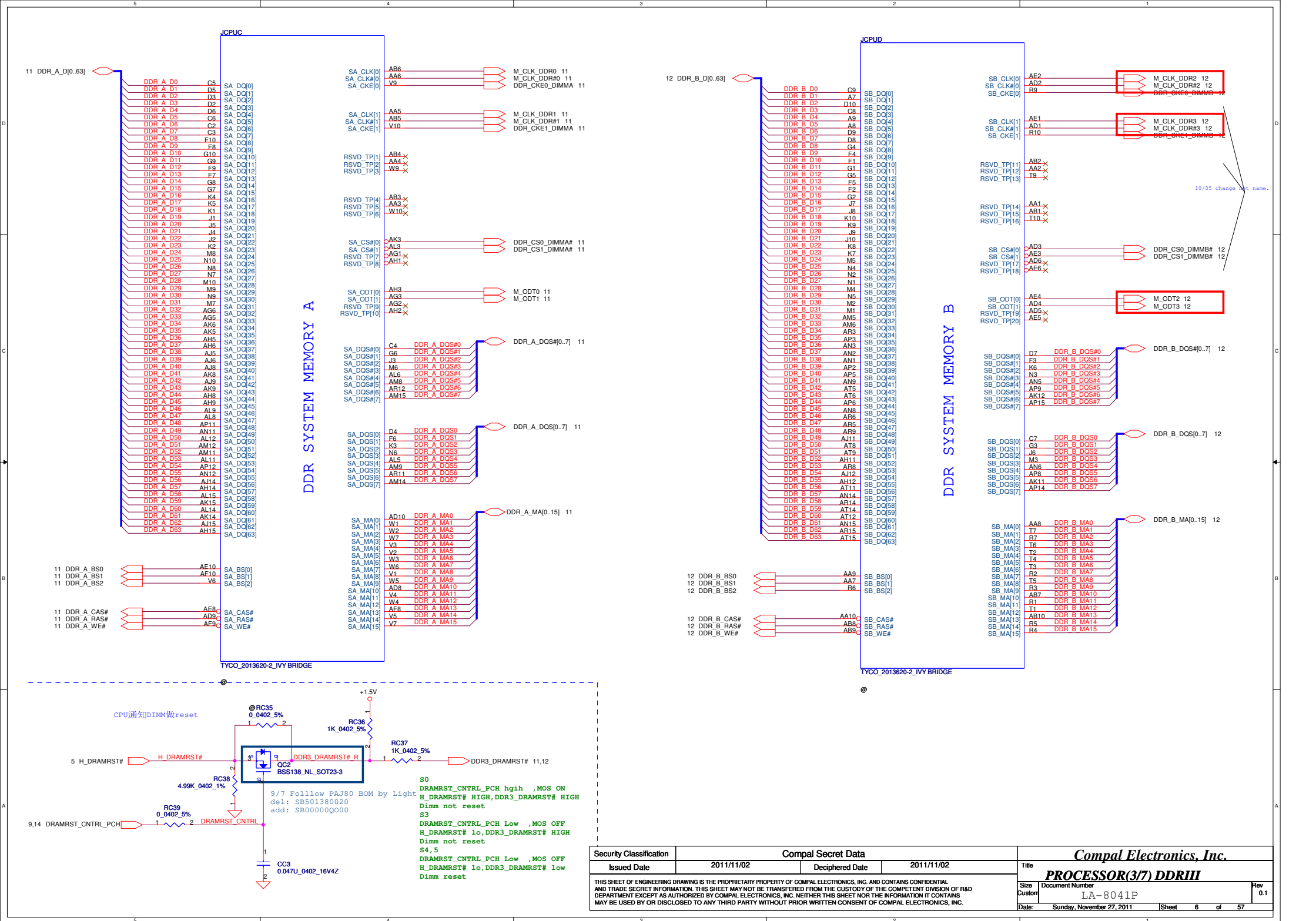
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

NOTE:eDP_COMPIO and eDP_ICOMPO should not be left floating even if Internal Graphic is disabled since they are shared with other interfaces



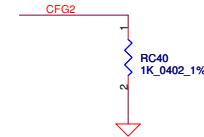
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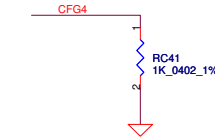
CFG Straps for Processor

change to install

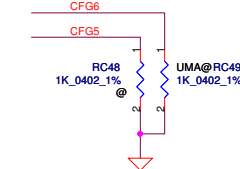


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>

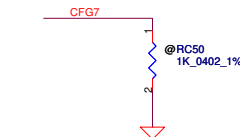
change to install



Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

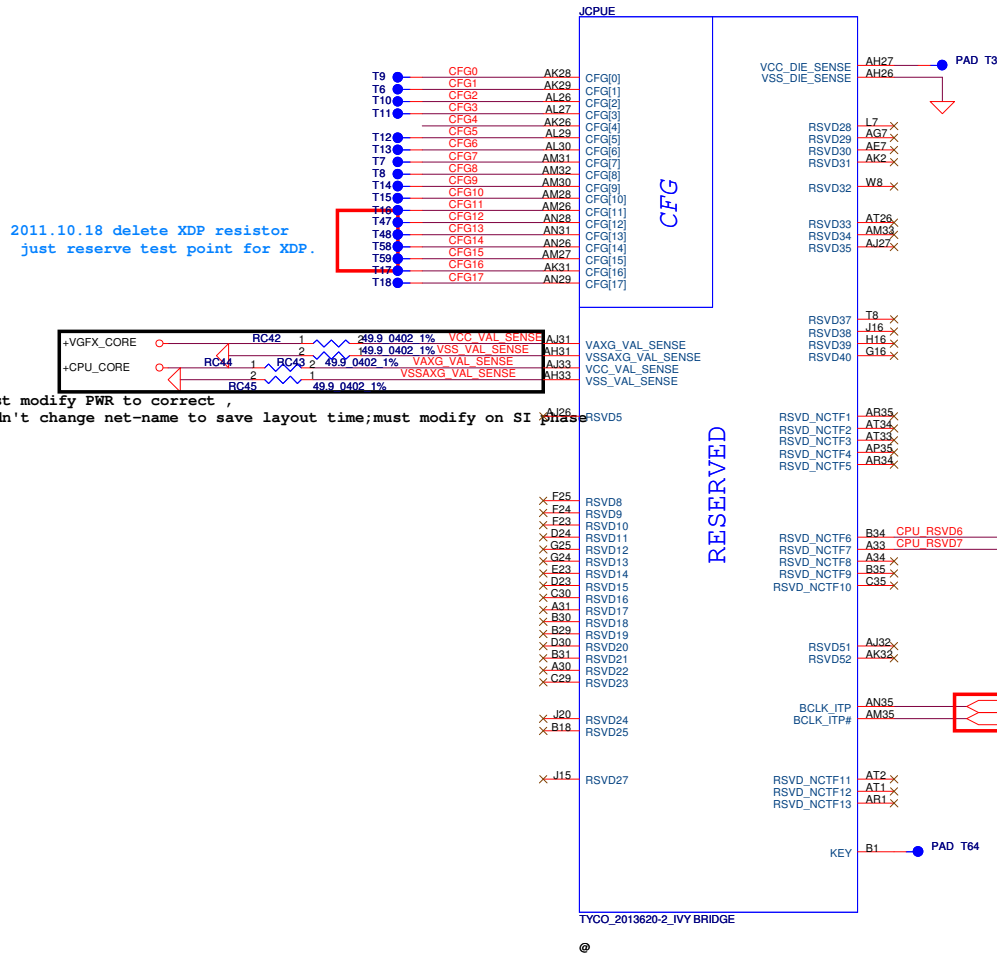


PCIE Port Bifurcation Straps	
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>★ 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>



PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

Change to part G.

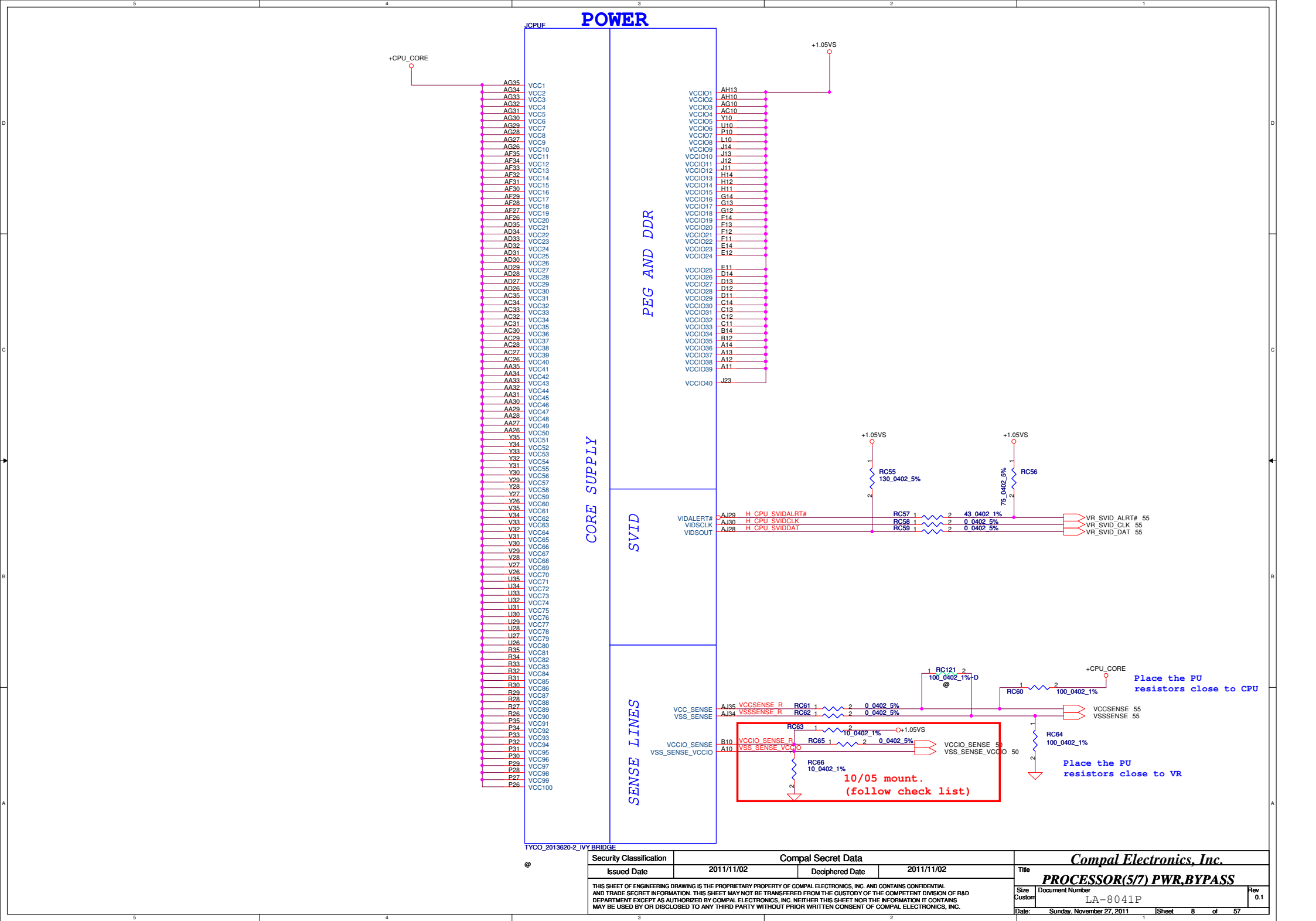


2011.10.18 delete XDP resistor just reserve test point for XDP.

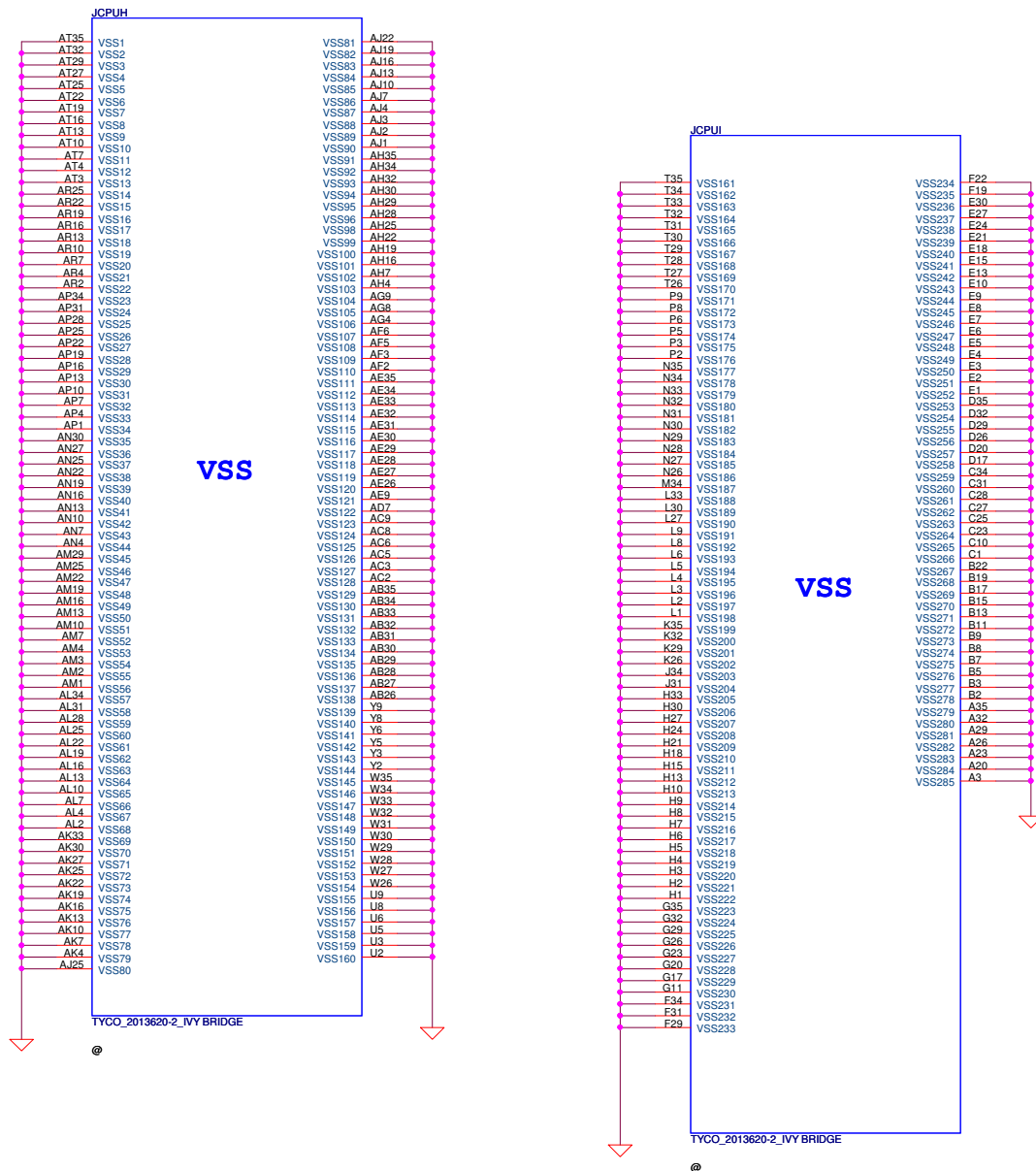
Just modify PWR to correct , didn't change net-name to save layout time; must modify on SI phase

ITP CLK change from part C.

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Title		PROCESSOR(47) RSVD,CFG			
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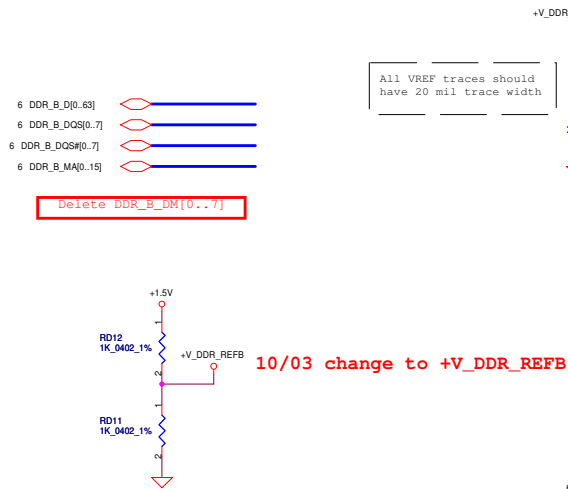
DDR3 SO-DIMM A



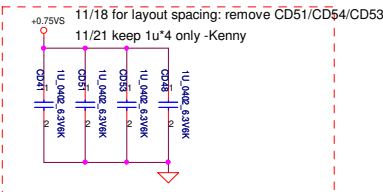
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DDR3 SO-DIMM B

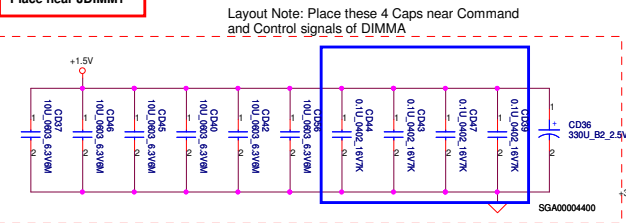
10/03 change to +V_DDR_REFB



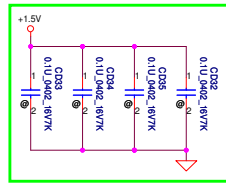
Layout Note:
Place near JDIMM1.203 & JDIMM1.204



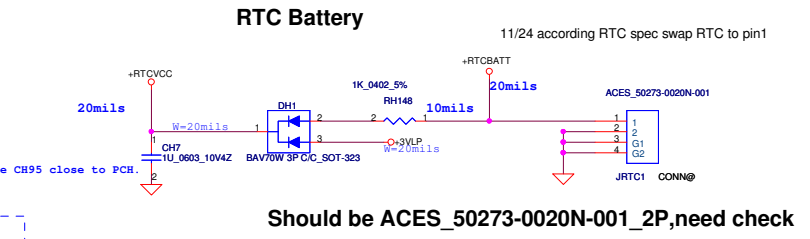
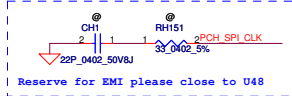
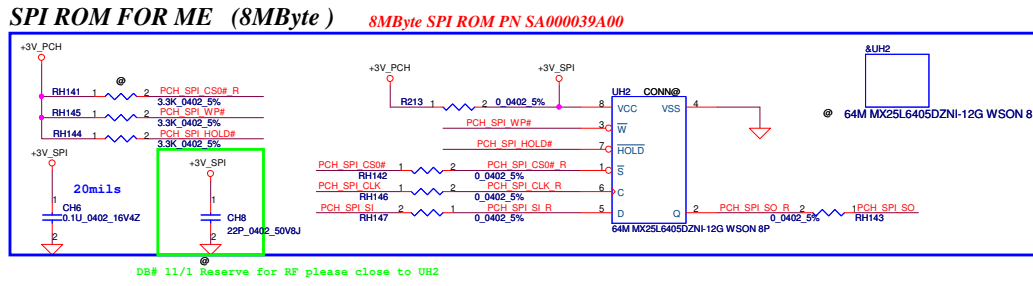
Layout Note:
Place near JDIMM1

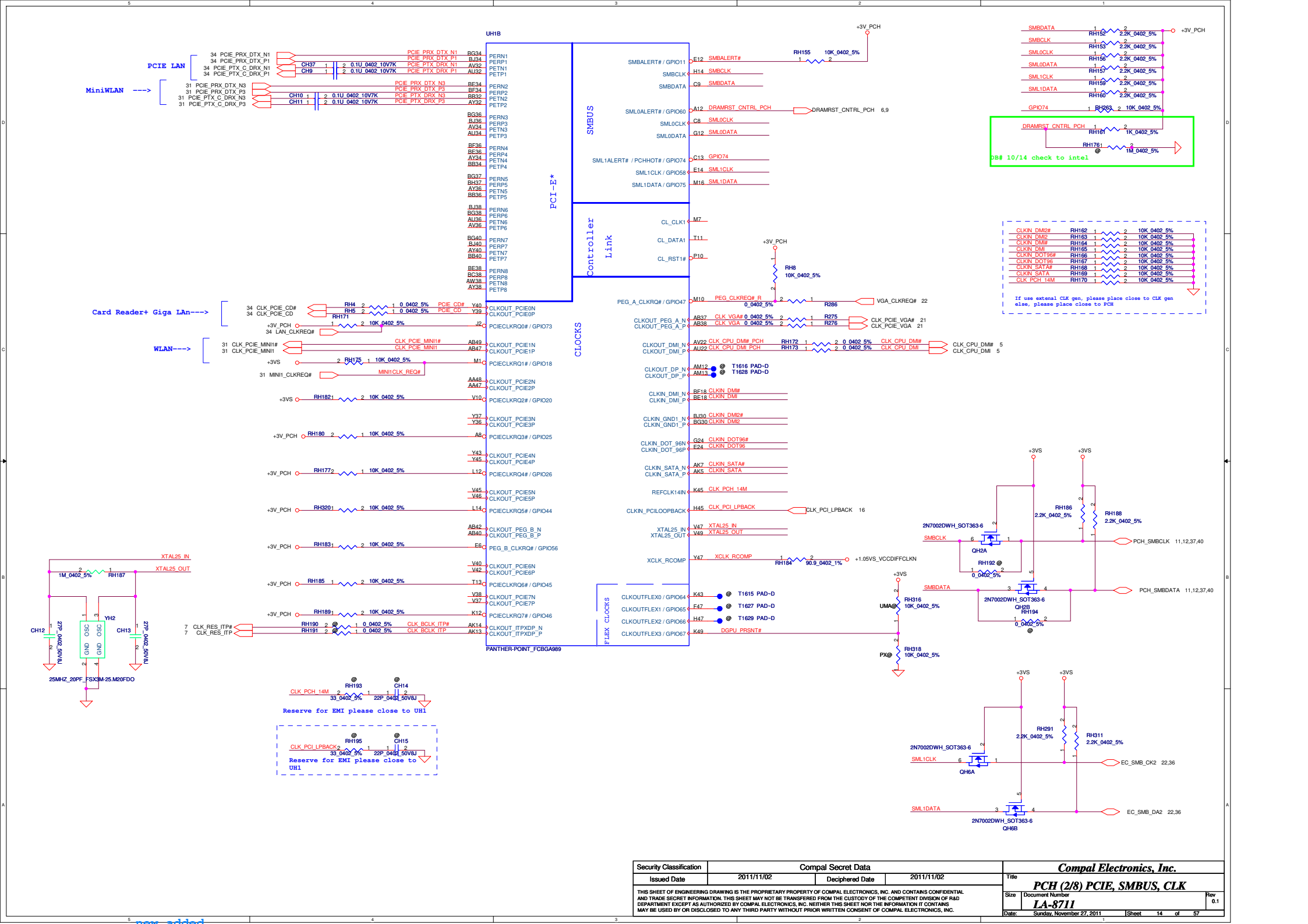


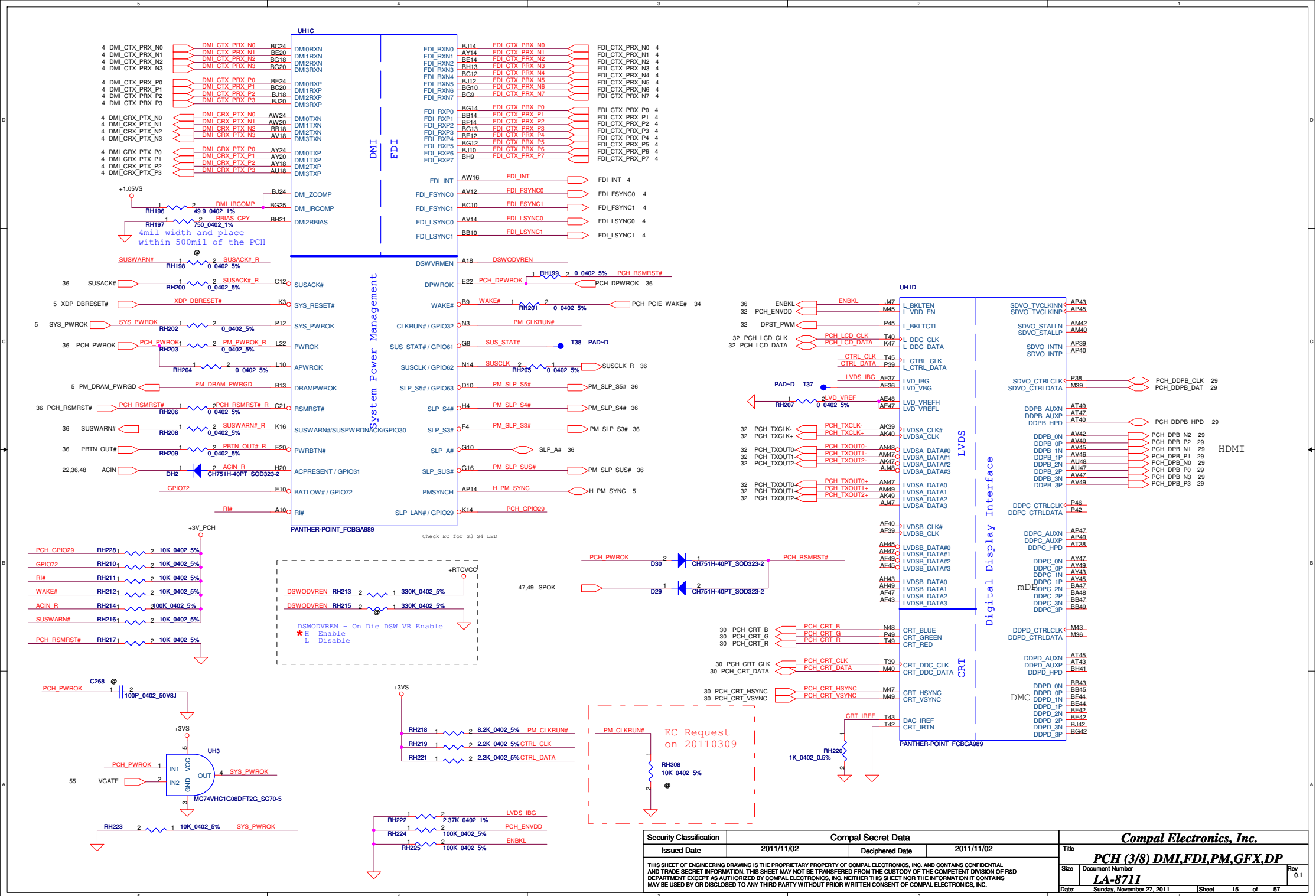
DDR3 SO-DIMM B

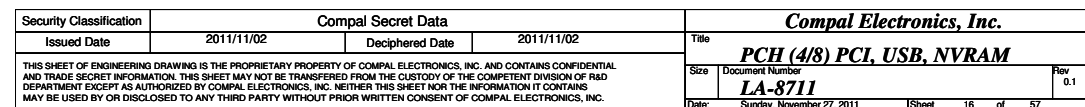


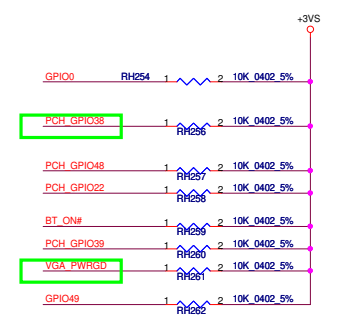
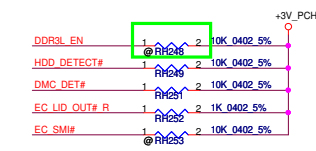
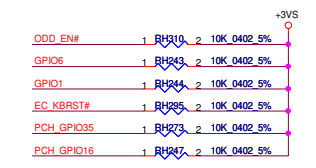
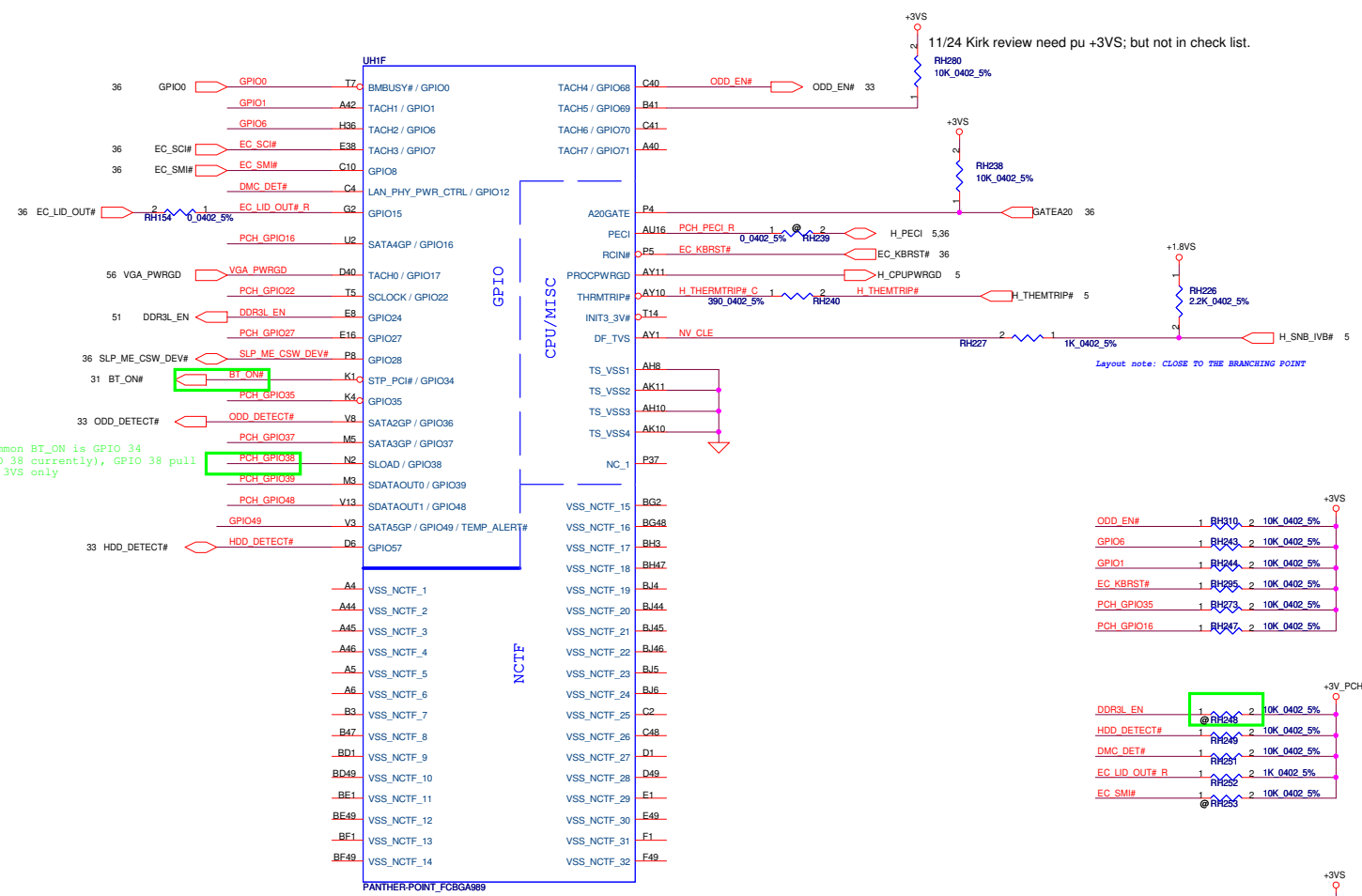
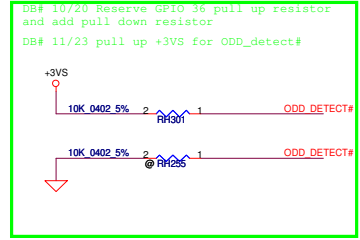
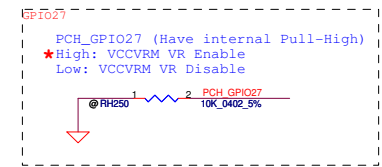
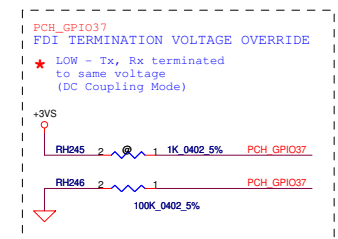
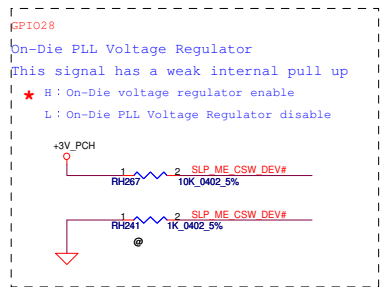
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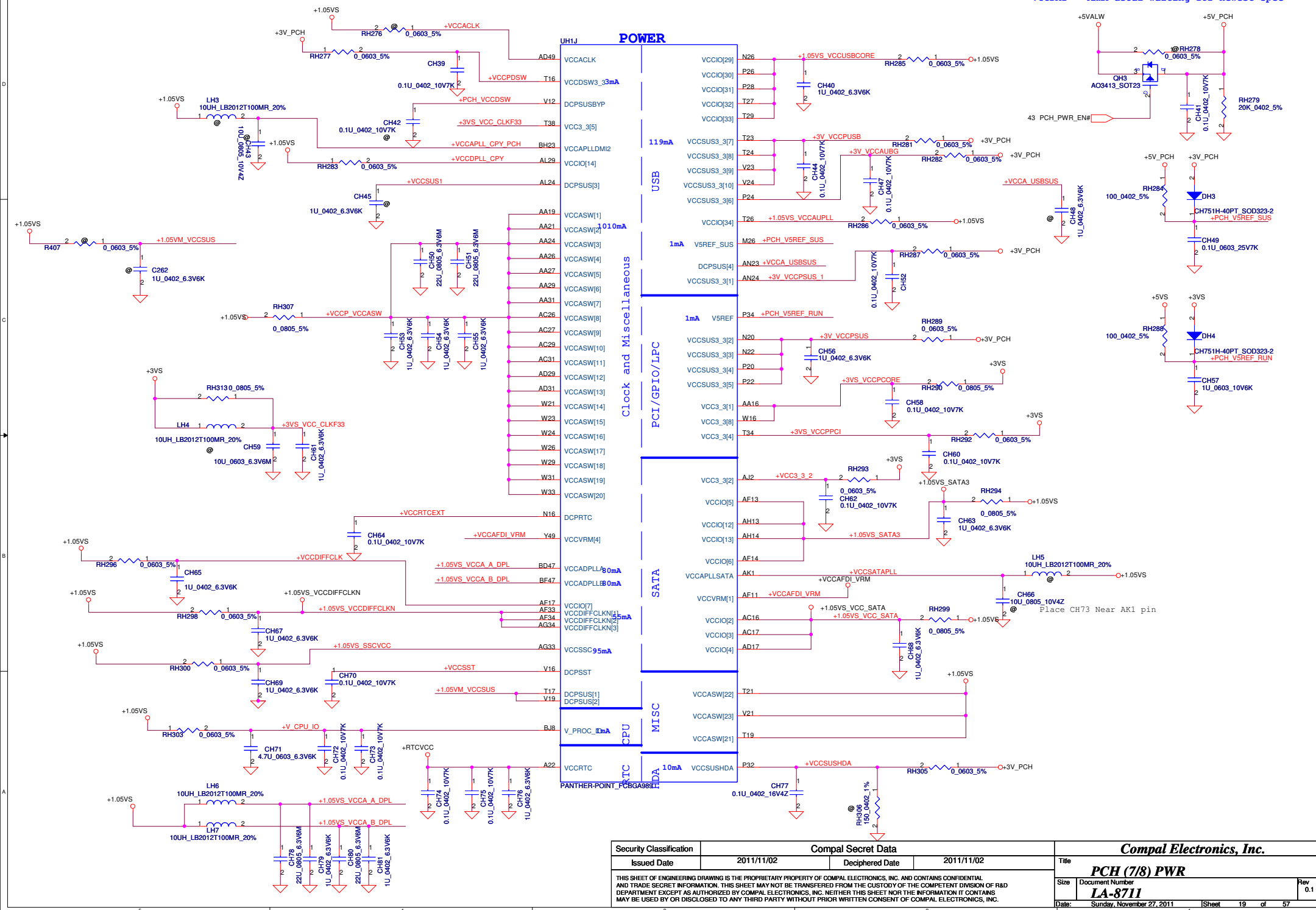




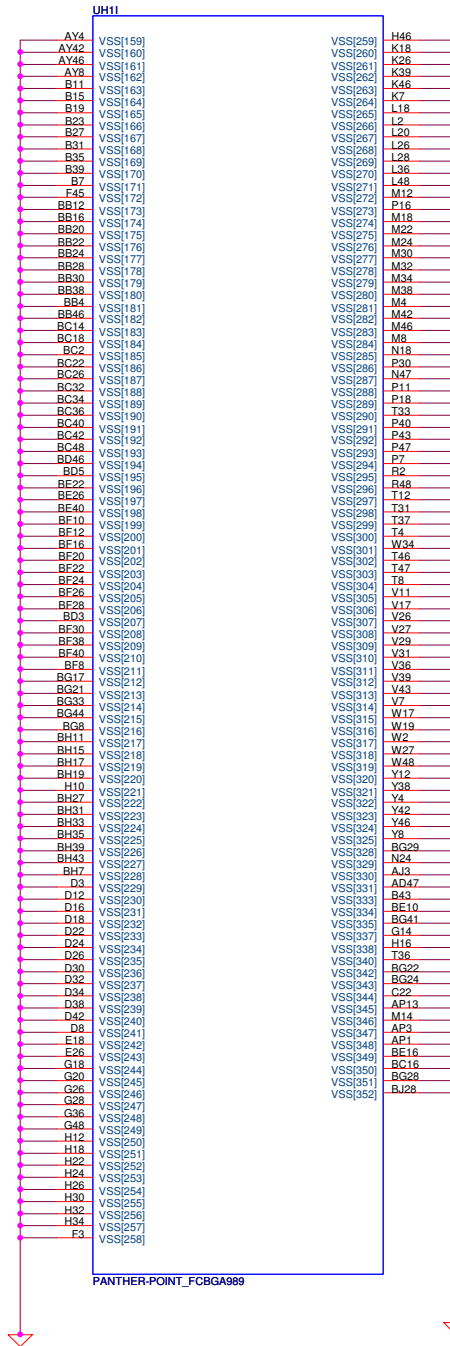
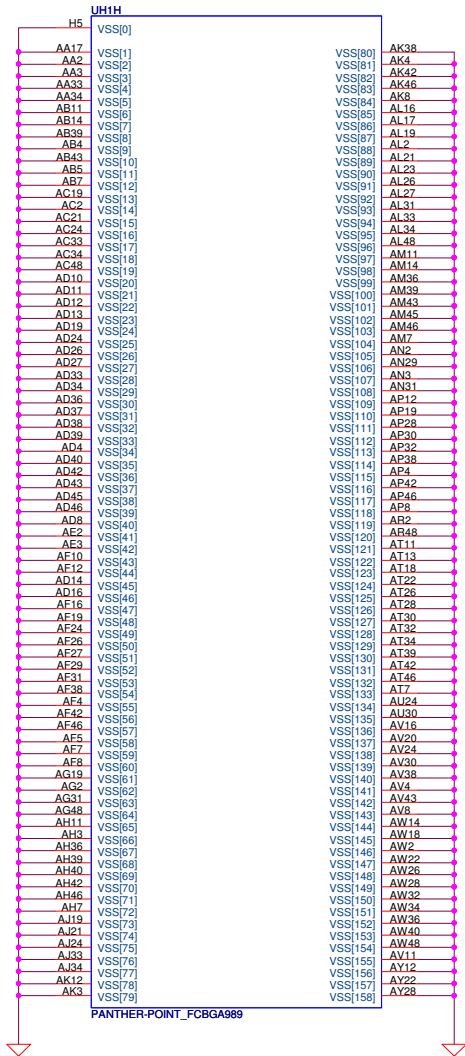


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VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

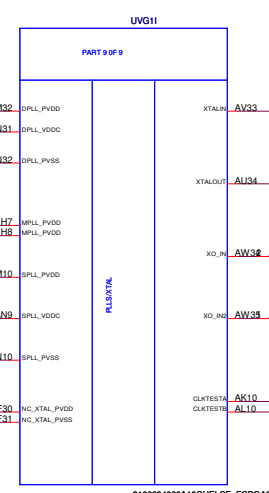
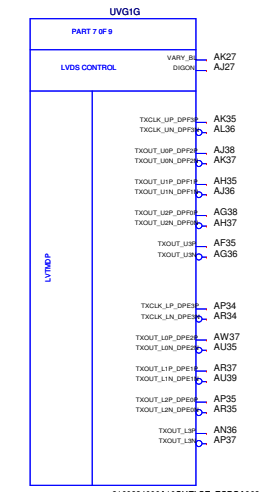
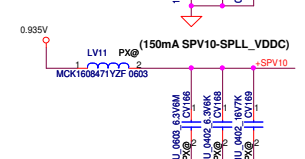
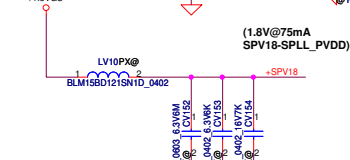
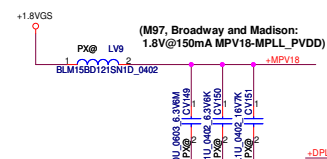
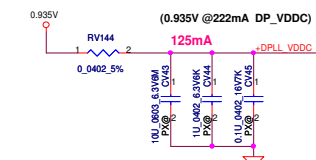
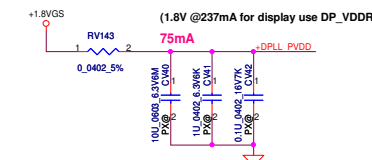
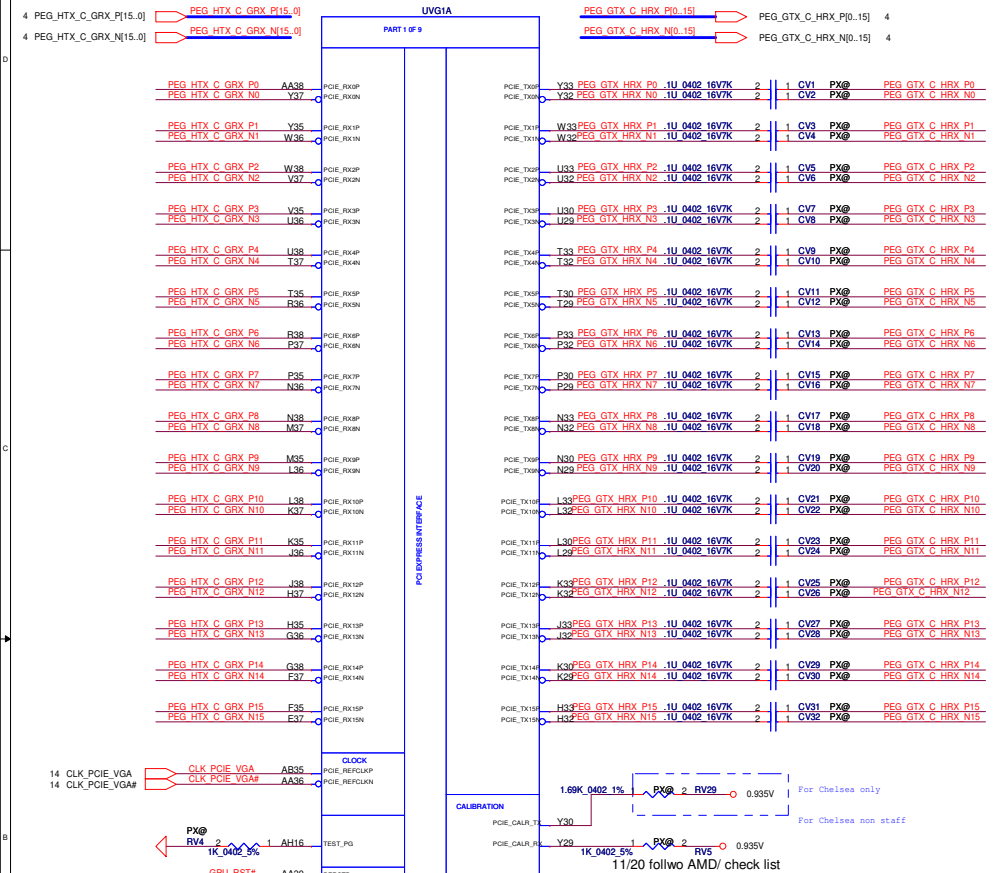


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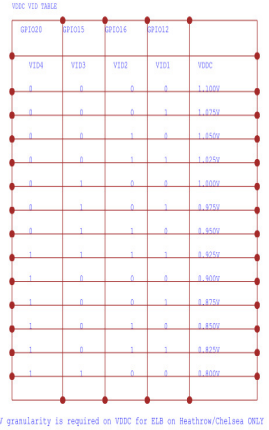
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LVDS Interface



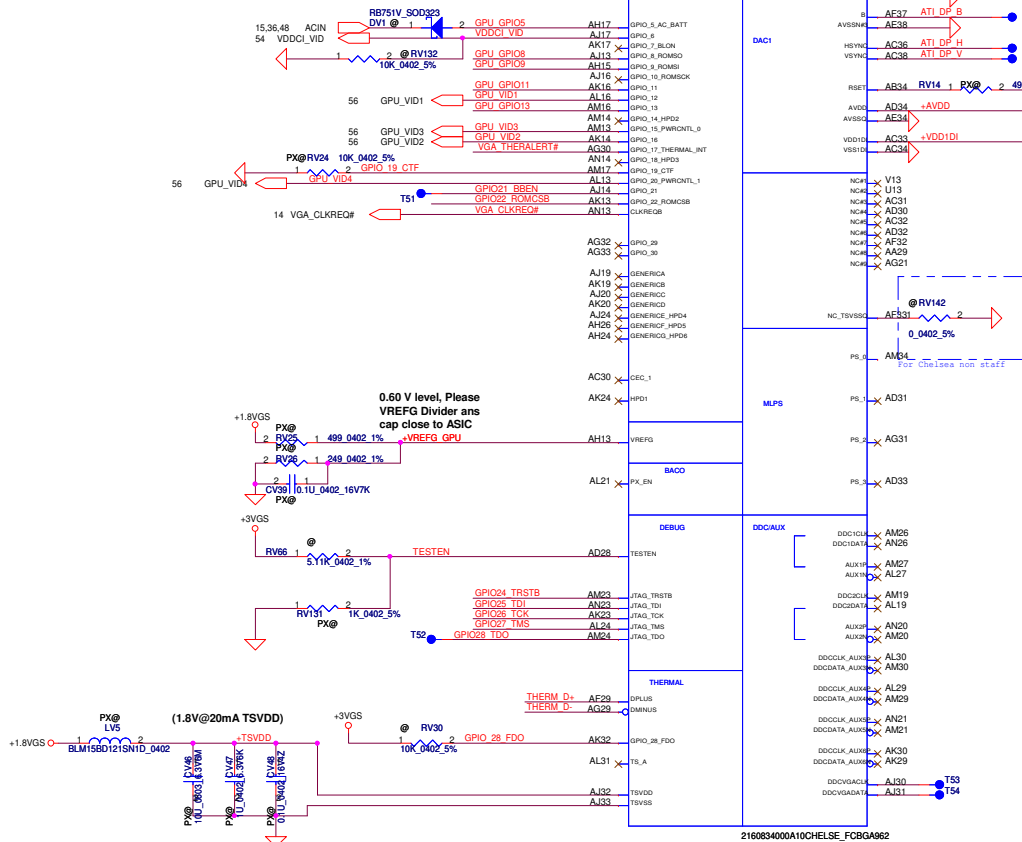
route 50ohms single-ended/100ohms diff and keep short Debug only, for clock observation, if not needed, DNI 5mil 5mil

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Size	C	Document Number	LA-8711	Rev
Date	Sunday, November 27, 2011	Sheet	21	of 57

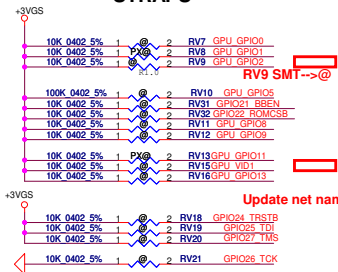


VRAM ID3

25mV granularity is required on VDDC for SLB on Beethrow/Chelona ONLY



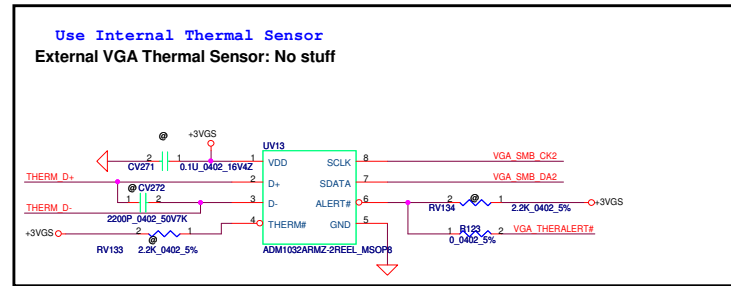
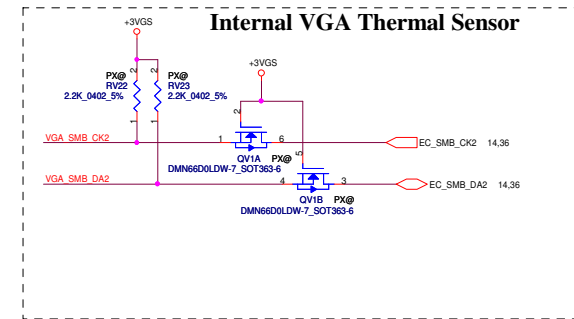
STRAPS



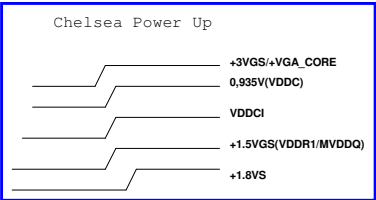
Update net name

CONFIGURATION STRAPS				RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS		
TX_PWRS_ENB	GPIO0	PCIE TRANSMITTER Power Saving Enable	0: 50% swing 1: Full swing	X	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X	
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.50T/s 1: 5.0T/s	0	
RSVD	GPIO8	Internal use only. This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected.		0	
RSVD	GPIO21			0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT GPIO13,12,11(config 2,1,0): internal PD. a) BIOS_ROM_EN=1, the config(2:0) defines the ROM type. b) BIOS_ROM_EN=0, the config(2:0) defines the primary aperture size of (3:0): 128MB 000 256MB 001 512MB 010	XXX		Memory apertures
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0	
BIF_VGA_DIS	GPIO9	VGA ENABLED		0	
RSVD	GENERICC			0	
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11	
AUD[0]	VSYSNC				
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET					
GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8	

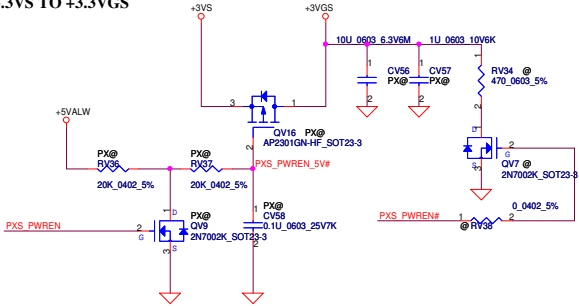
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



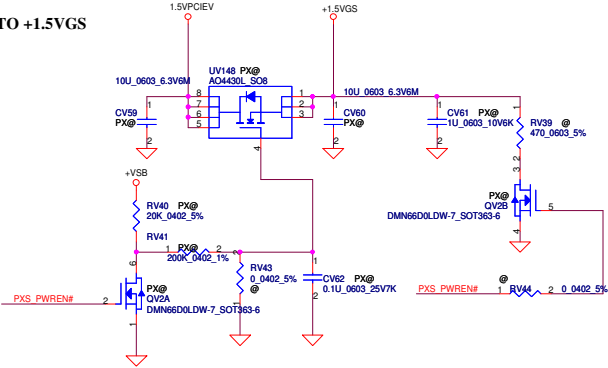
Name	FCH Pin Assignments
FE_GPIO0	GPIO191
FE_GPIO1	GPIO192
FE_PWRGD	GPIO28



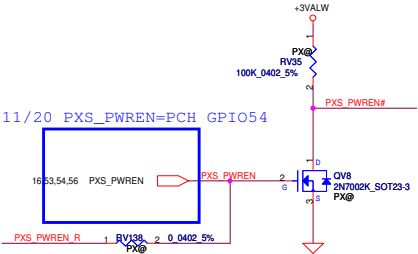
+3.3VS TO +3.3VGS



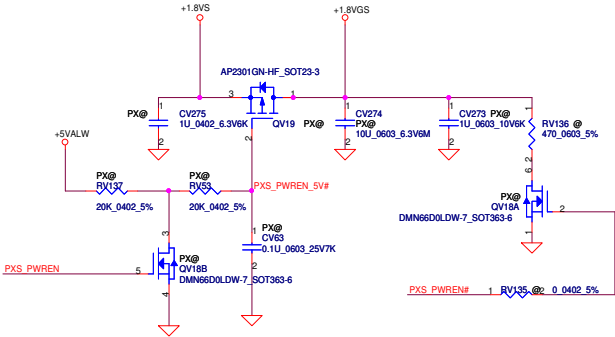
+1.5V TO +1.5VGS

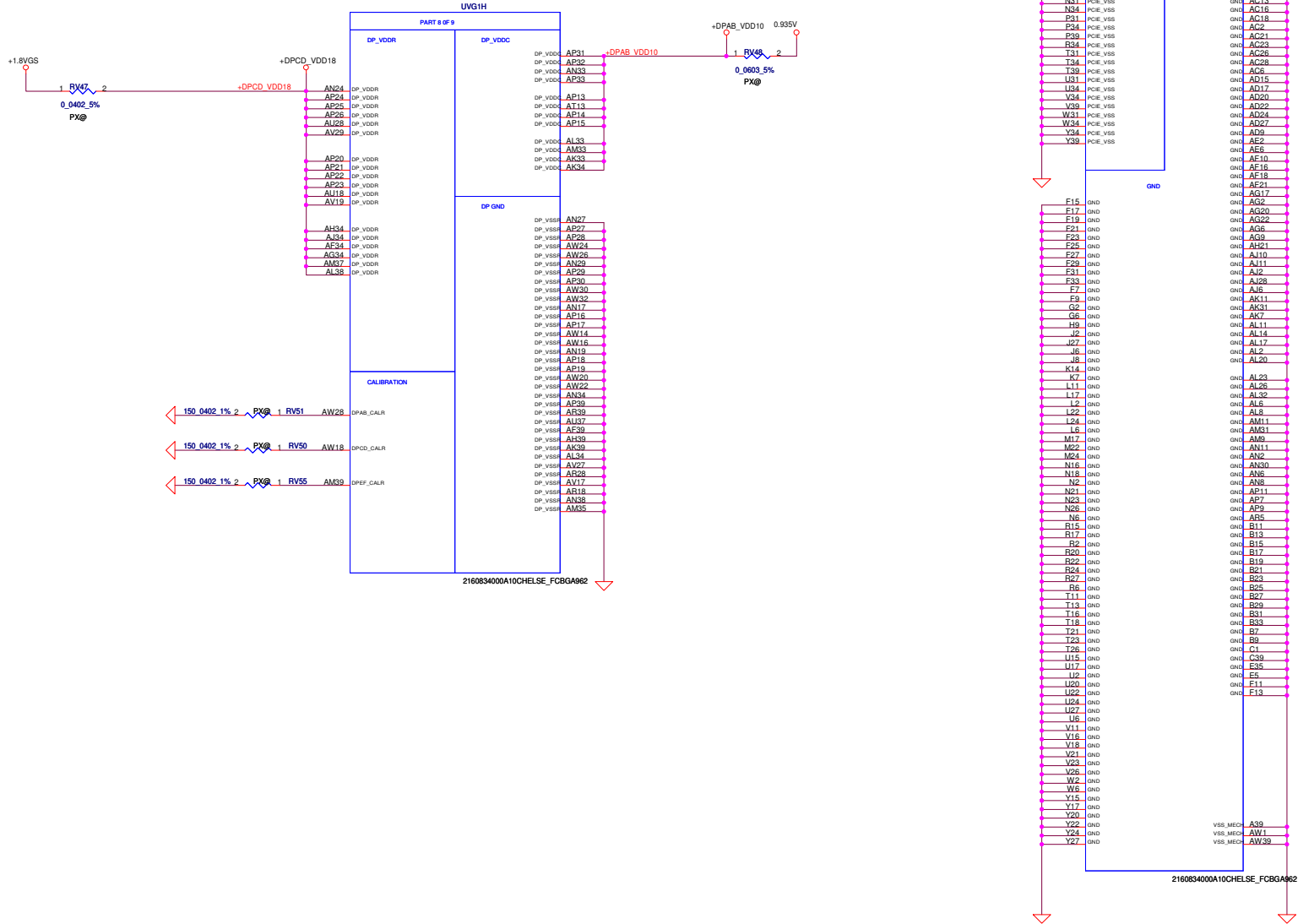


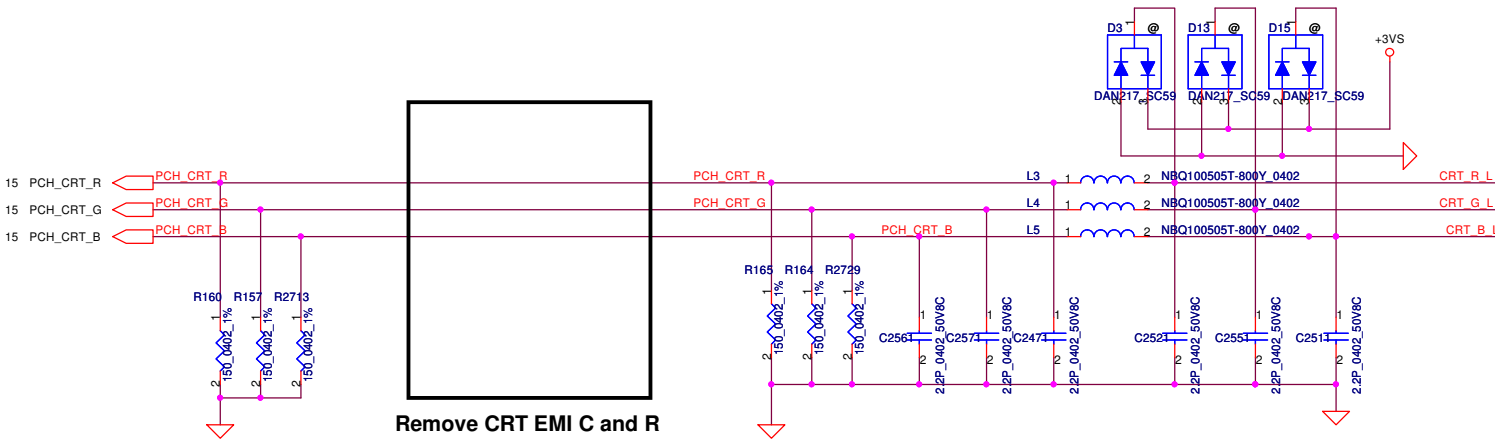
11/20 PXS_PWREN=PCH GPIO54



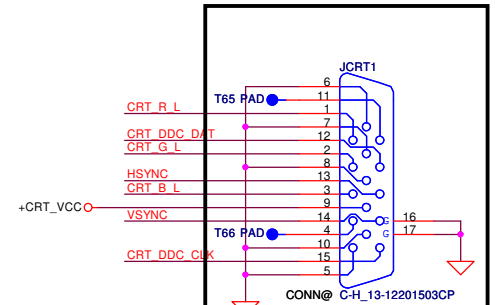
+1.8VS TO +1.8VGS



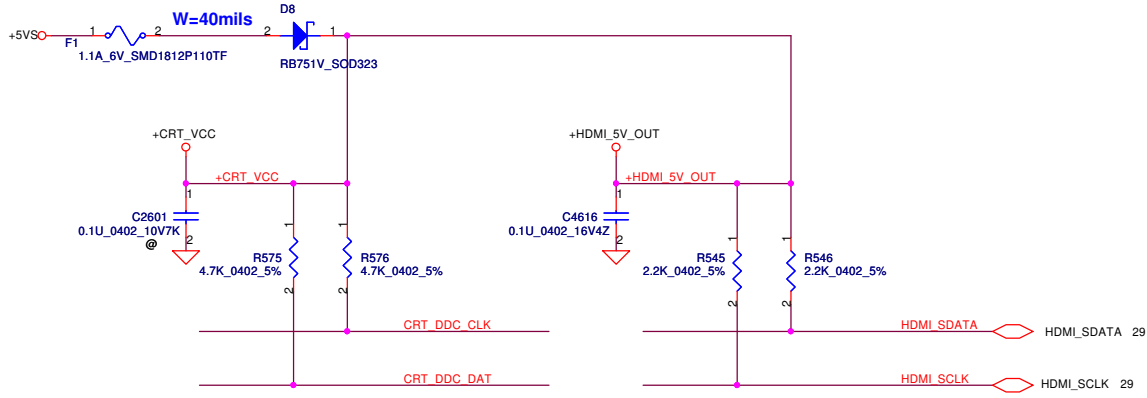
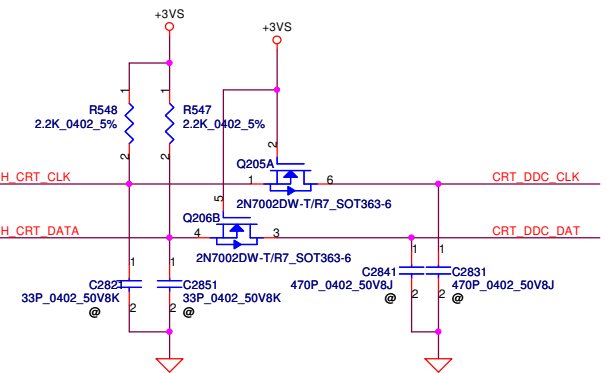
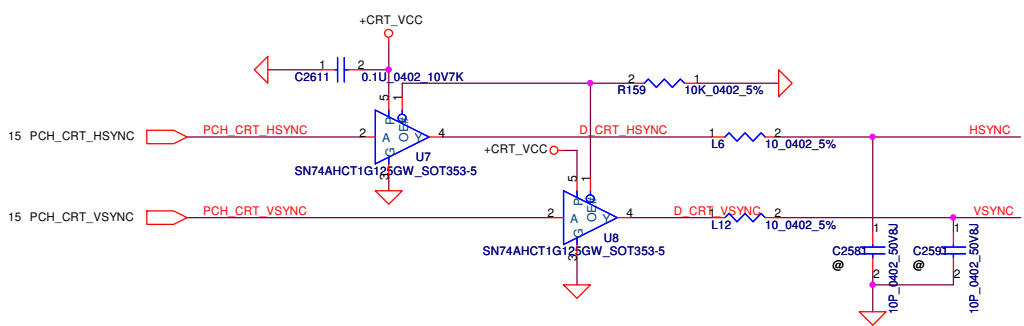




CRT CONNECTOR



USE old footprint need update
C-H_13-12201503CP_15P-T



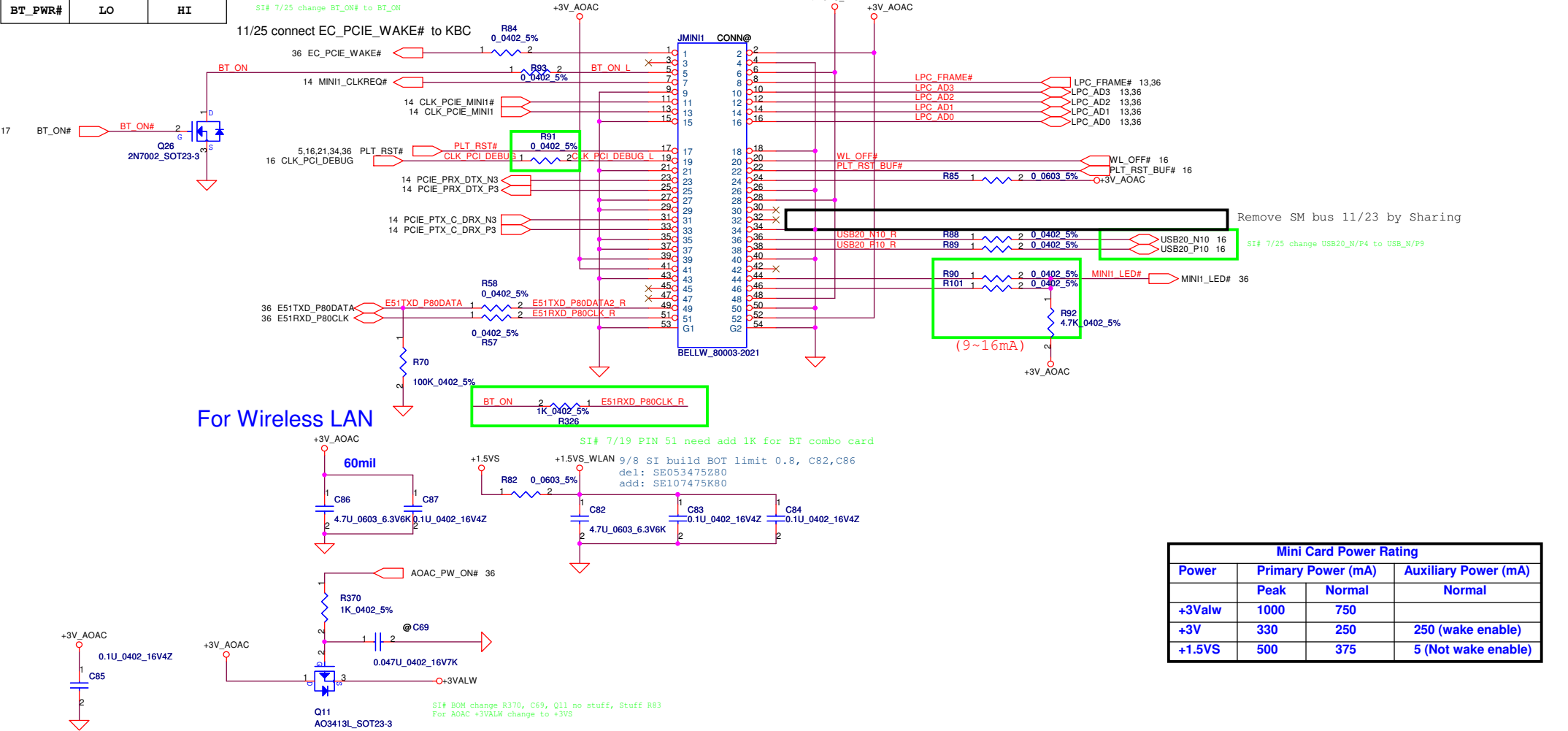
For CRT

For HDMI

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								Size	Document Number	
								LA-8711		0.1
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WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

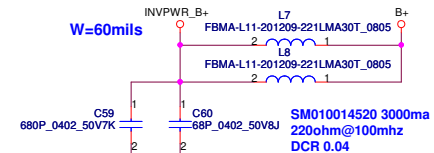
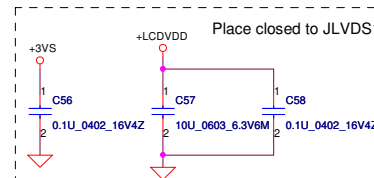
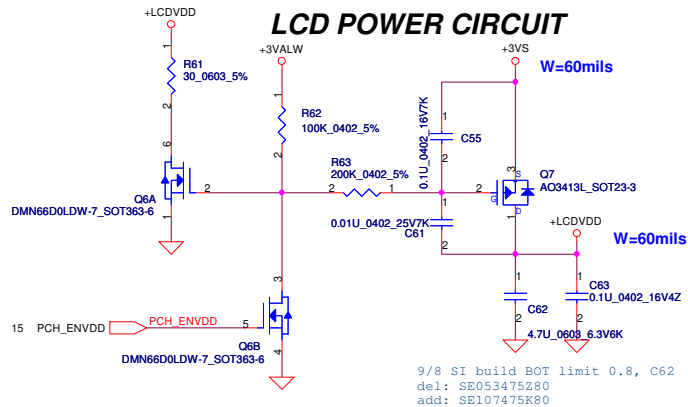


For Wireless LAN

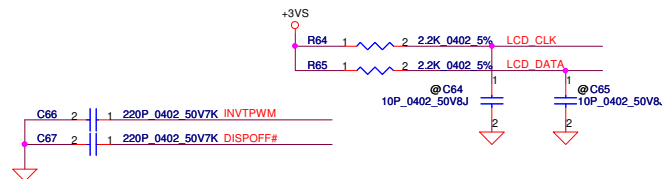
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3Valw	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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				Size Document Number
				LA-8711
				Rev 0.1
				Date: Sunday, November 27, 2011
				Sheet 31 of 57

SI# 8/15 R62 change to +3VALW, R61change to 10 ohm, R63 change to 200K ohm

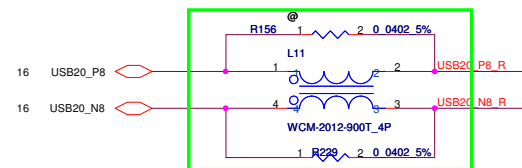
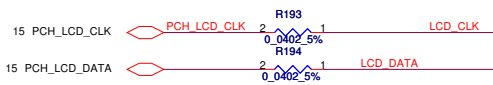
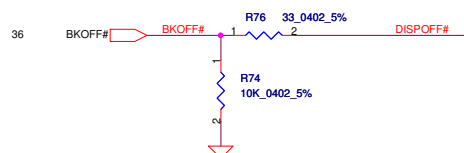
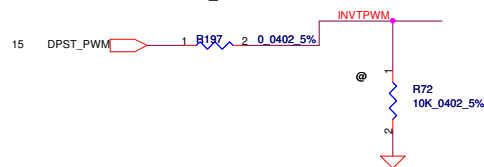


LCD/LED PANEL Conn.

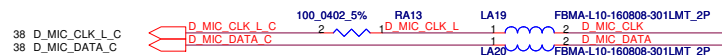
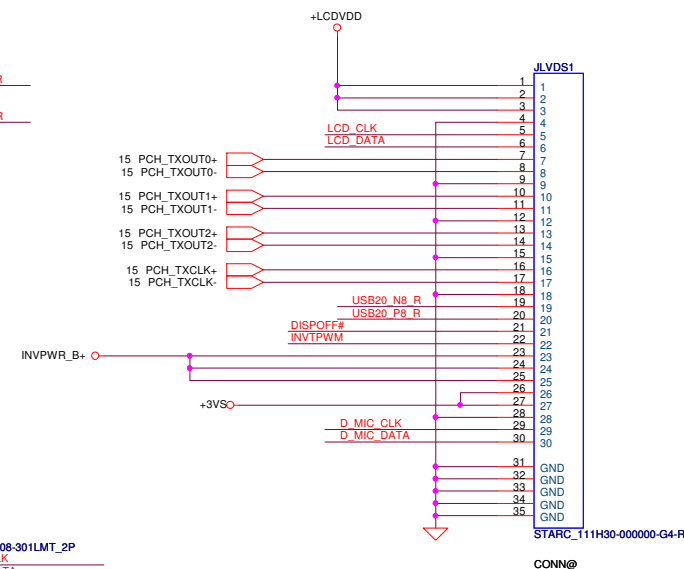
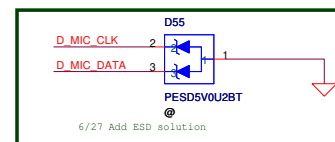


Check pin definition.

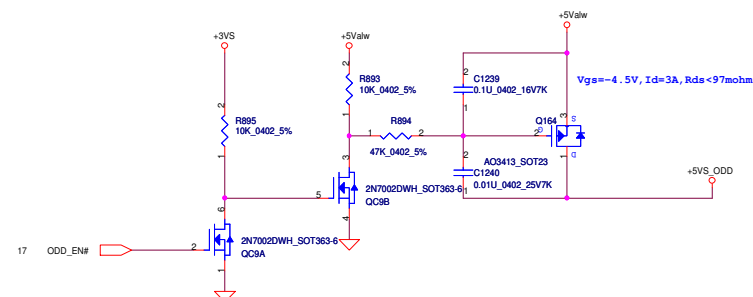
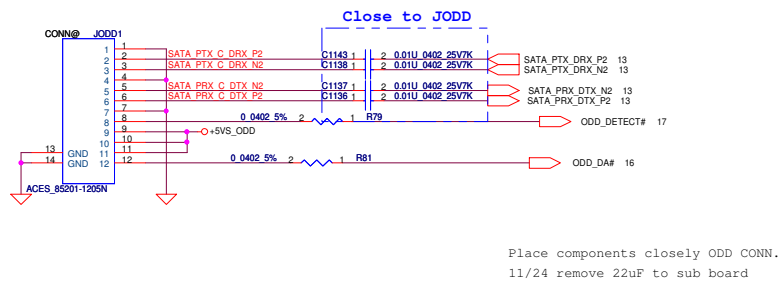
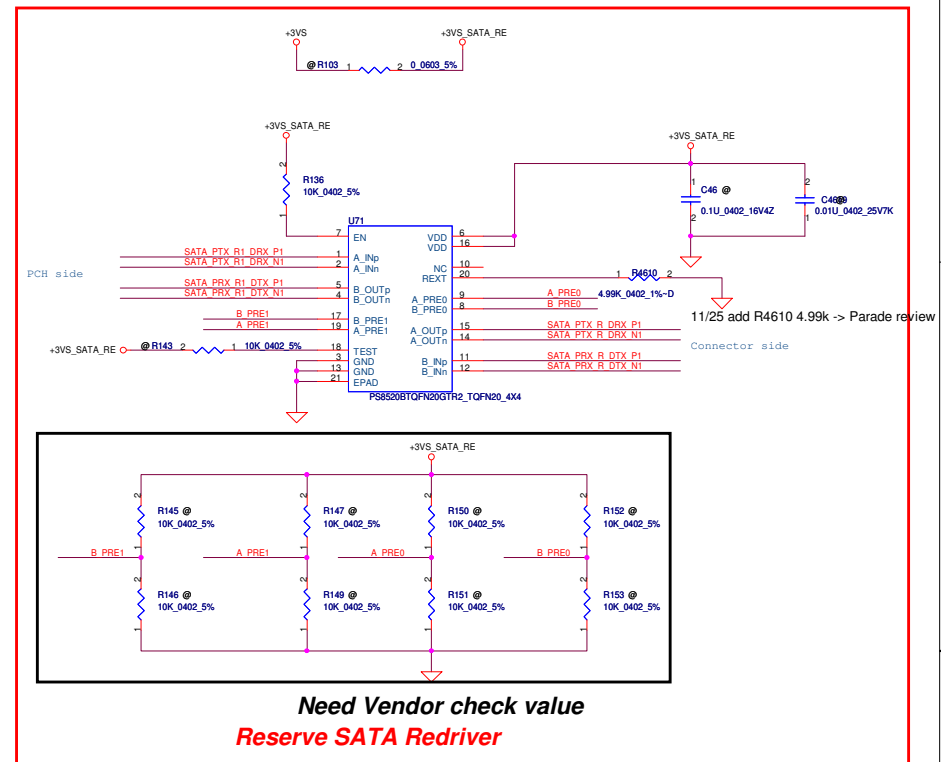
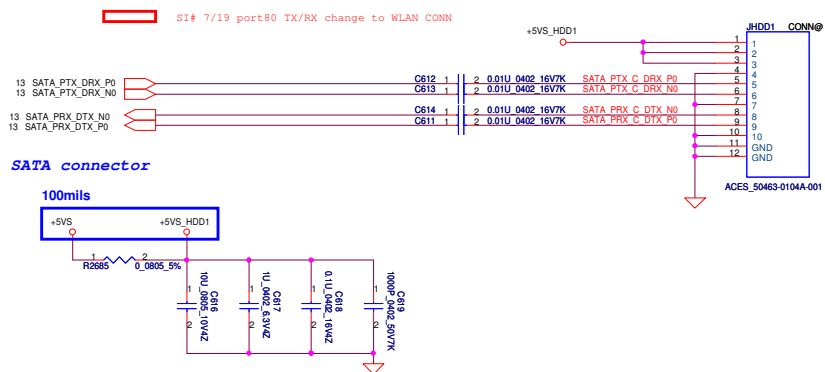
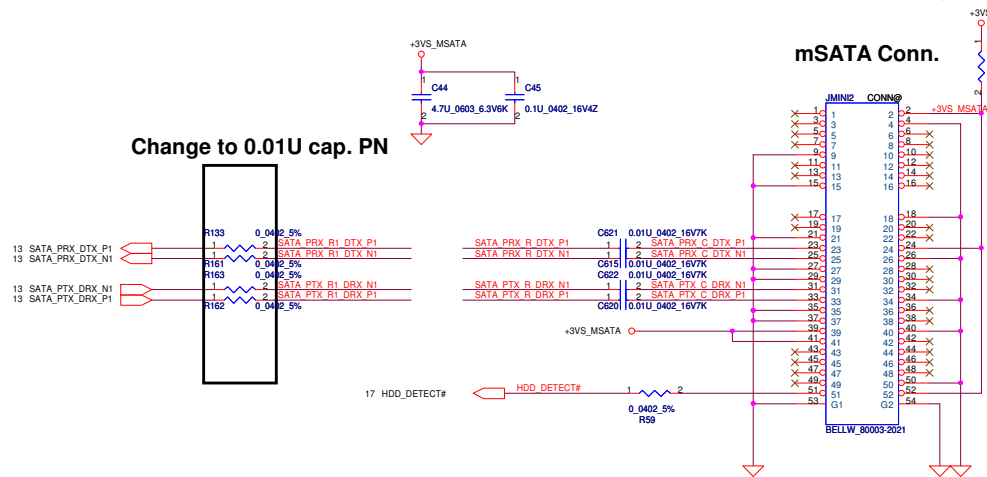
11/23 remove INVT_PWM



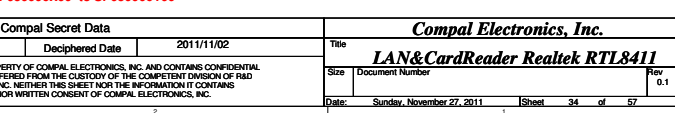
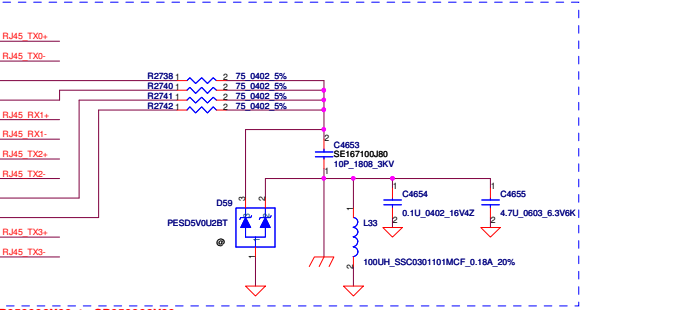
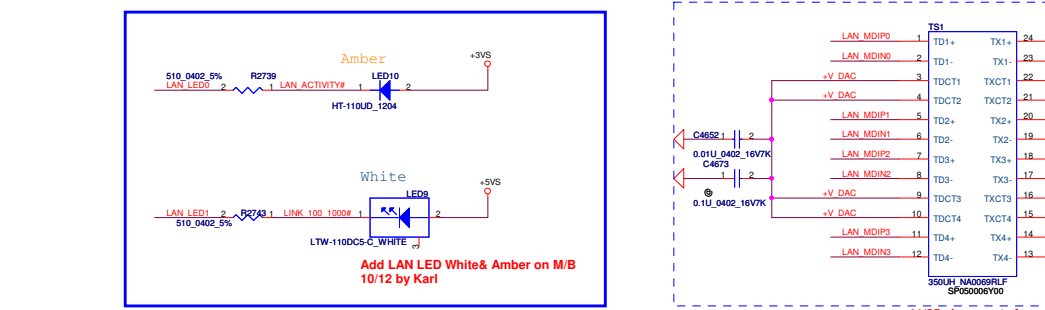
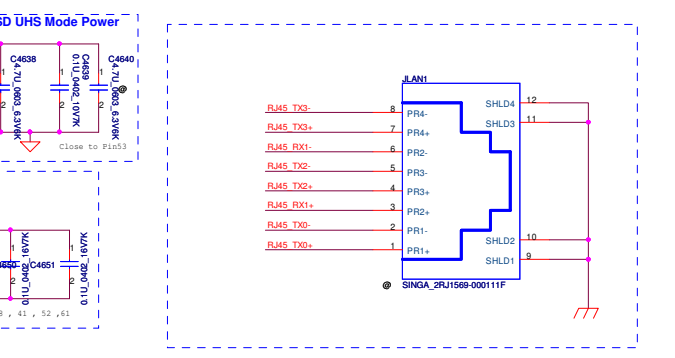
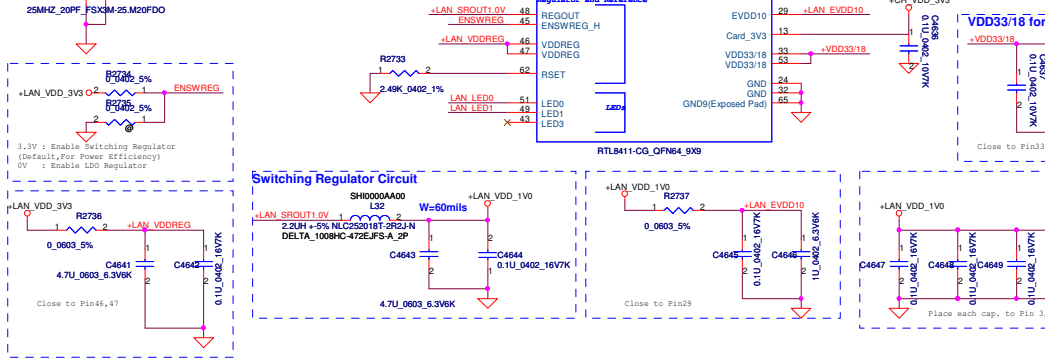
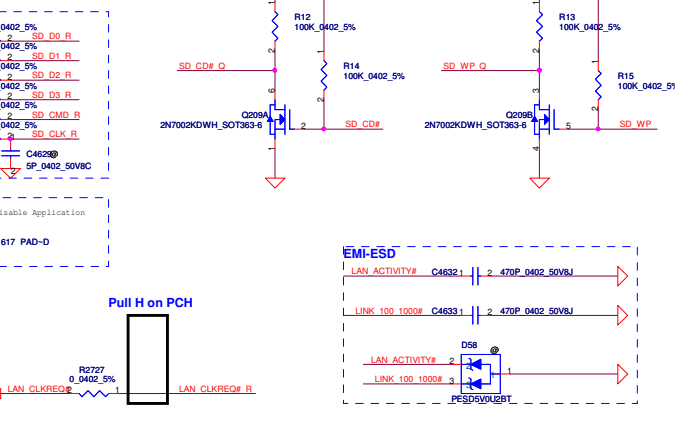
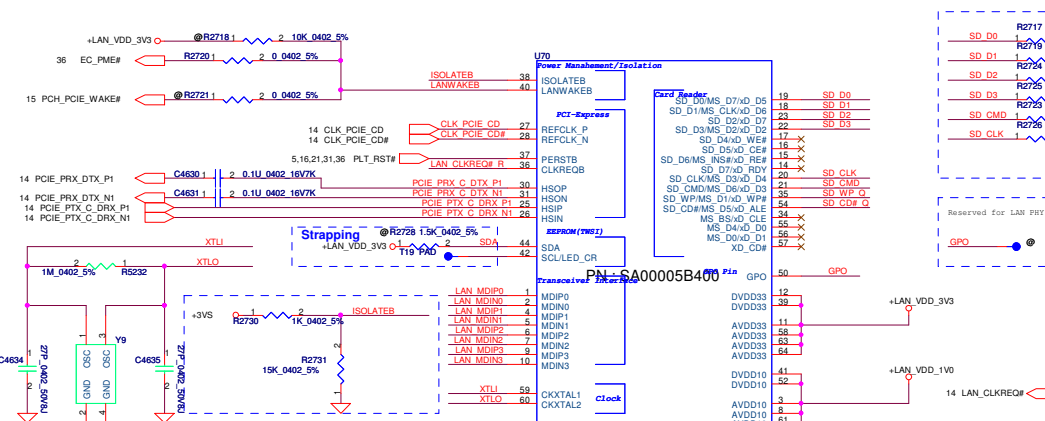
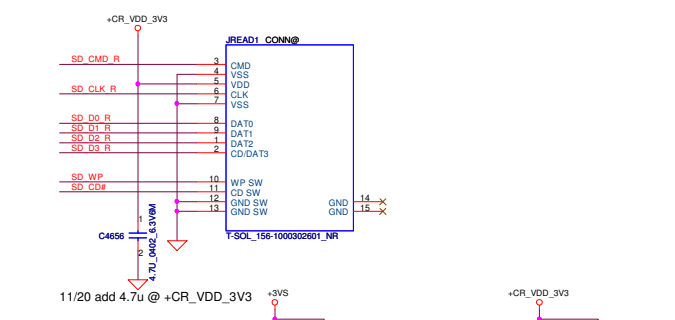
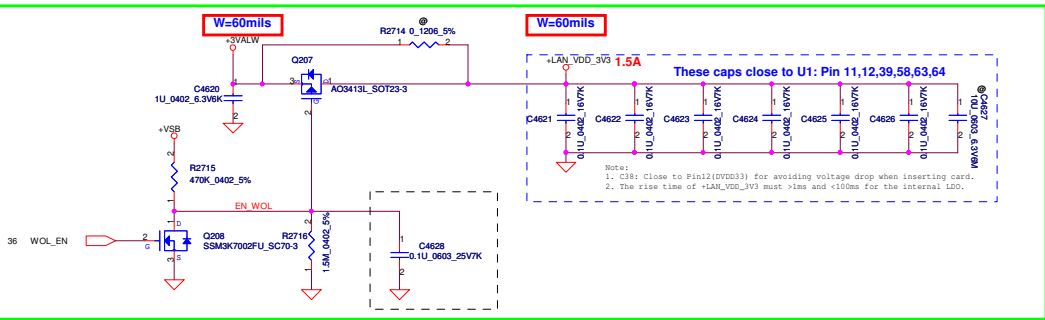
8/19 change stuff L26 by EMI request



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								Size	Document Number			Rev		
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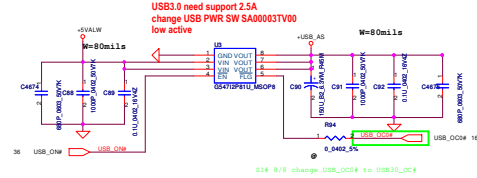
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				mSATA Connector	
				Size C	Document Number LA-8711
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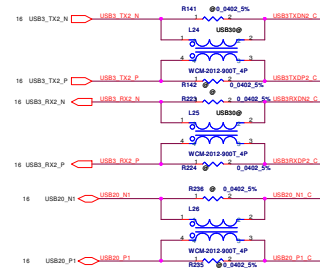
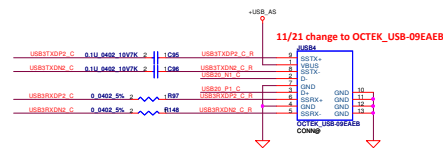
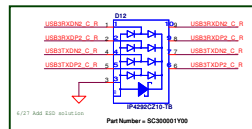
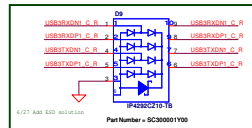
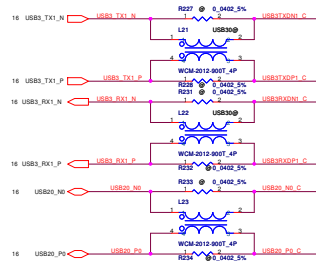
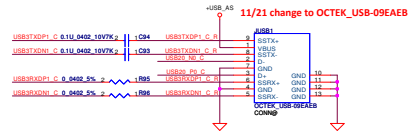
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				Size	Document Number
				Date	Sunday, November 27, 2011
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USB3.0

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

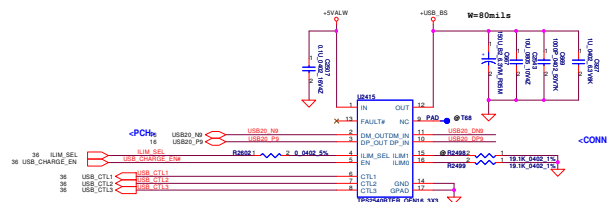


S1# 8/8 change USB_OC0# to USB30_OC#

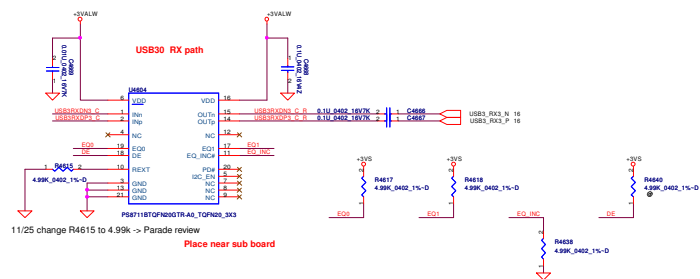


USB2.0 charger

USB charger footprint need change to TPS2543

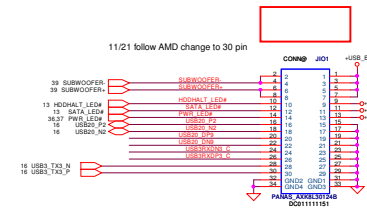


State	S0	S3, S4, S5
Mode	CDP	DCP
Control pin	CTL1 CTL2 CTL3 ILIM_SEL	CTL1 CTL2 CTL3 ILIM_SEL
	1 1 X 1	0 0 1 1



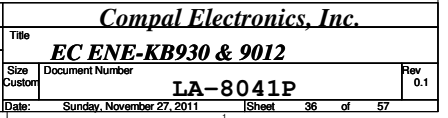
11/25 change R4615 to 4.99k -> Parade review

Place near sub board

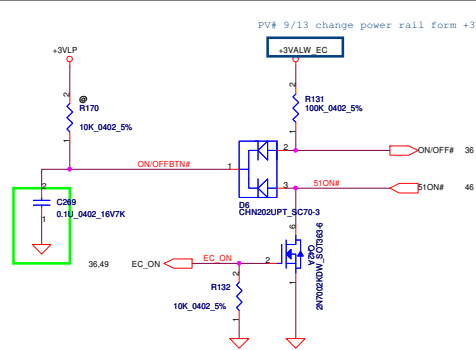


11/21 follow AMD change to 30 pin

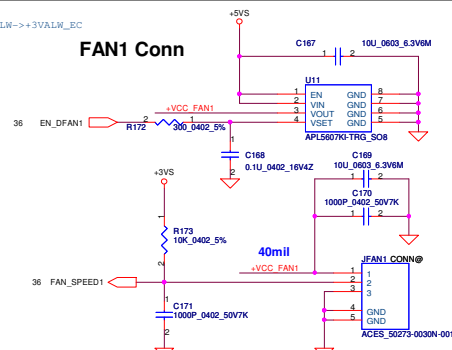
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Issued Date	2011/1/02	Deciphered Date	2011/1/02	USB Con & Daughter Con	
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				LA-9041P	
			Date	Monday, November 27, 2011	Sheet 25 of 17



PV# 9/13 change power rail form +3VALW->+3VALW_EC

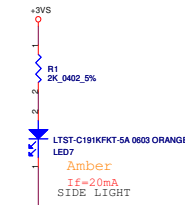
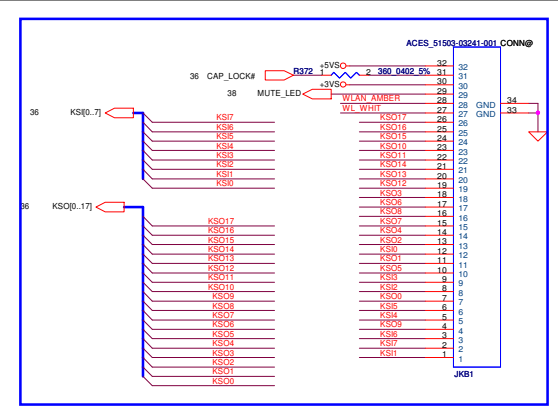


FAN1 Conn



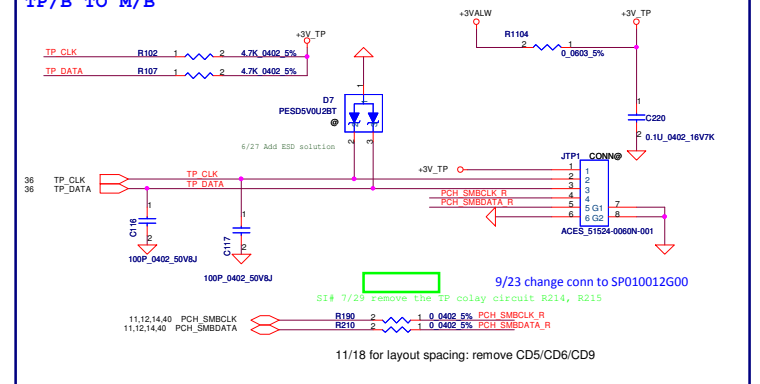
KSO17	C247	1	2	100P	0402	50V6J
KSO16	C251	1	2	100P	0402	50V6J
KSO15	C252	1	2	100P	0402	50V6J
KSO14	C227	1	2	100P	0402	50V6J
KSO13	C228	1	2	100P	0402	50V6J
KSO12	C229	1	2	100P	0402	50V6J
KSO11	C231	1	2	100P	0402	50V6J
KSO10	C232	1	2	100P	0402	50V6J
KSO9	C233	1	2	100P	0402	50V6J
KSO8	C234	1	2	100P	0402	50V6J
KSO7	C235	1	2	100P	0402	50V6J
KSO6	C236	1	2	100P	0402	50V6J
KSO5	C237	1	2	100P	0402	50V6J
KSO4	C238	1	2	100P	0402	50V6J
KSO3	C239	1	2	100P	0402	50V6J
KSO2	C240	1	2	100P	0402	50V6J
KSO1	C241	1	2	100P	0402	50V6J
KSO0	C250	1	2	100P	0402	50V6J

6/27 add 33 ohm and 22p by EMI request



36 TP_ON_OFF_LED# TP_ON OFF LED#

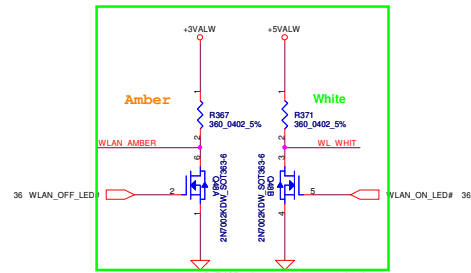
TP/B TO M/B



9/23 change conn to SP010012G00

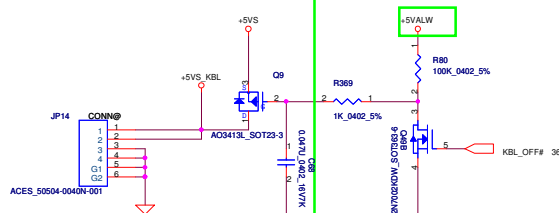
SI# 7/25 remove the TP colay circuit R214, R215

11/18 for layout spacing: remove CD5/CD6/CD9

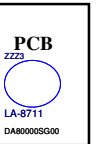
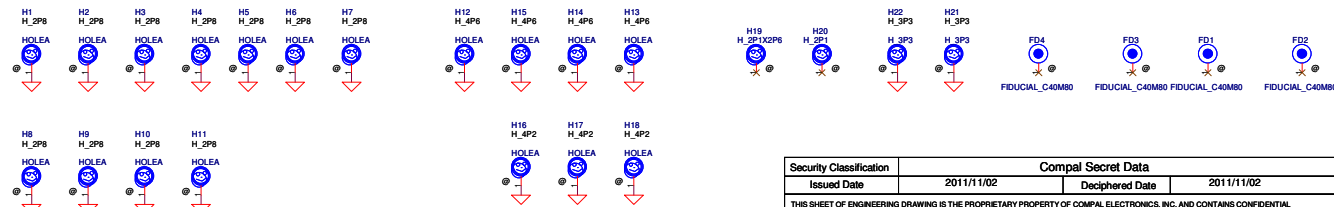
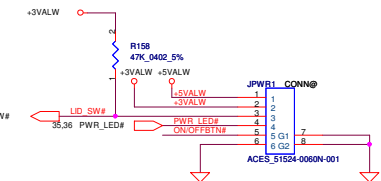


SI# 7/25 Change WLAN LED design

Keyboard backlight Conn



SI# 7/25 Add Q49B for K/B back light level shifter



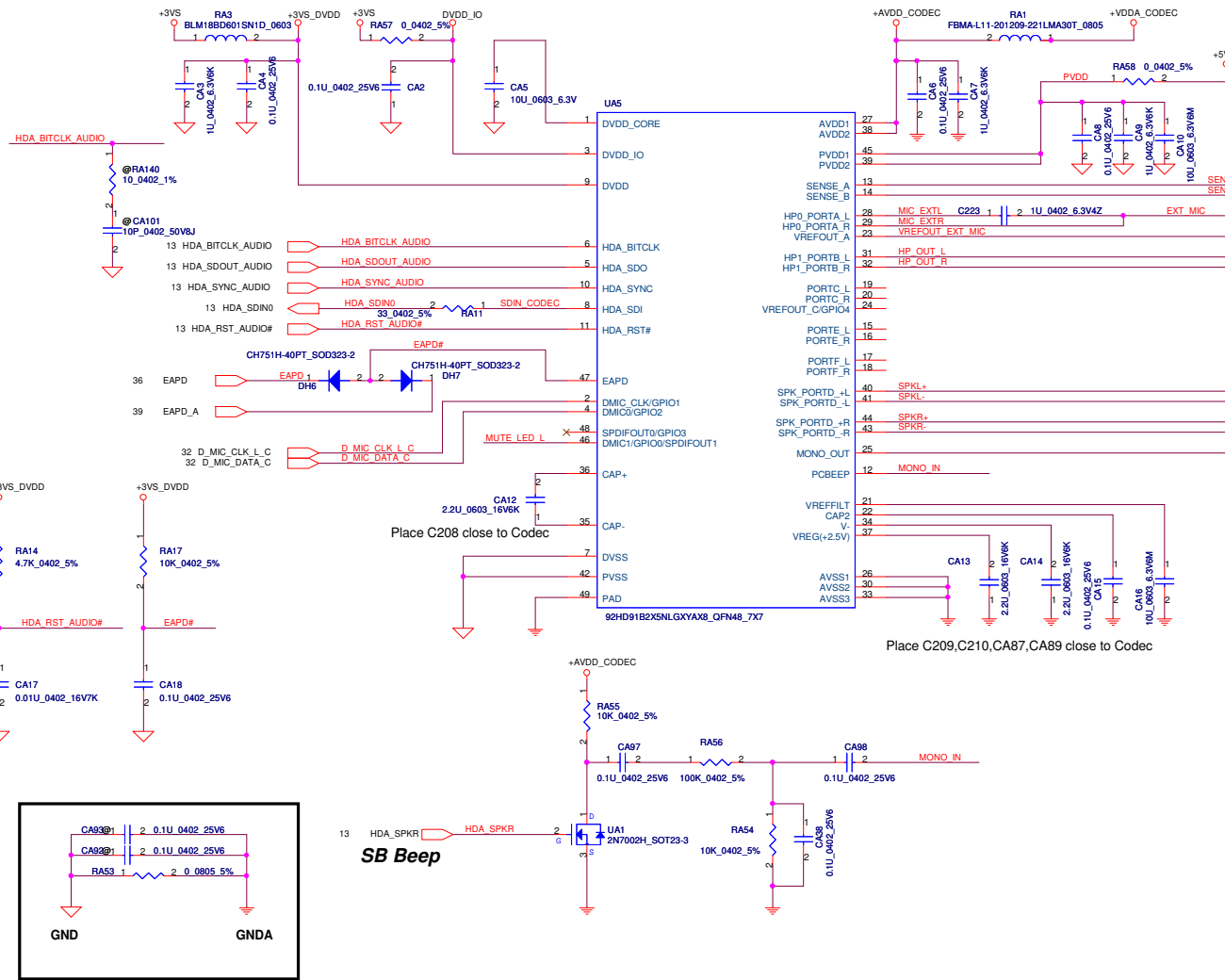
Security Classification	Compal Secret Data	
Issued Date	2011/11/02	Deciphered Date
		2011/11/02
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Title		KB/TP/LED/FAN/Screw/Gsensor
Size	Document Number	Rev
Custom	LA-8041P	8.1
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DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Place AVDD ,PVDD,and DVDD capacitor close to Codec

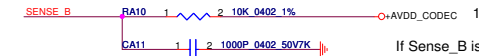
Notes:

Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than
6 inches, change C12 to 0.1uF



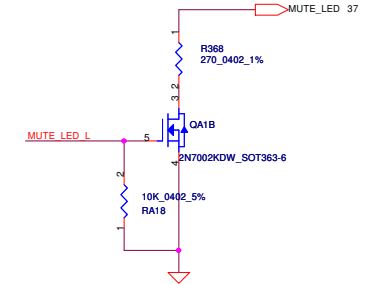
11/21 RA10 change to 10K(un-used)

PLACE CLOSE TO U1 PIN 14

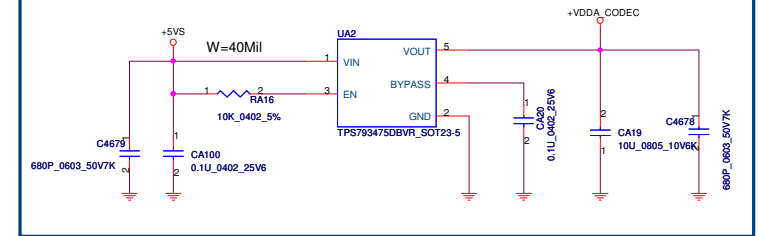
If Sense_B is un-used, then pull high
Sense_B to AVDD by 10Kohm resistor

HP Jack
Ext MIC

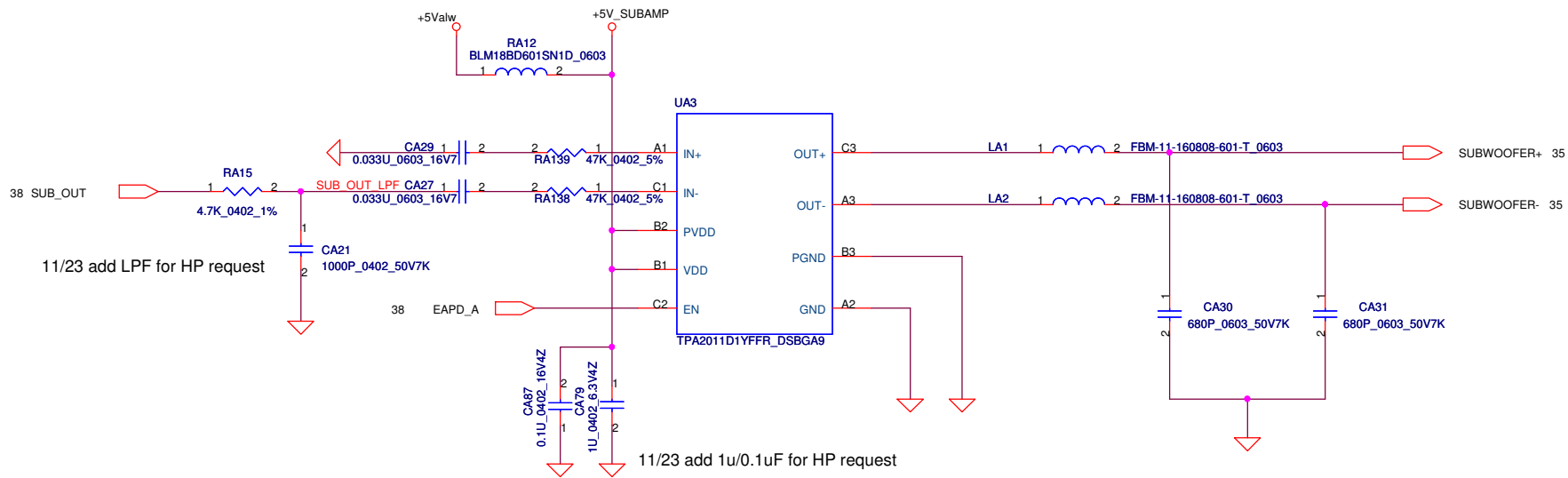
Internal SPKR
(front stereo speaker)



9/27 LDO TPS793475DBVR for audio power



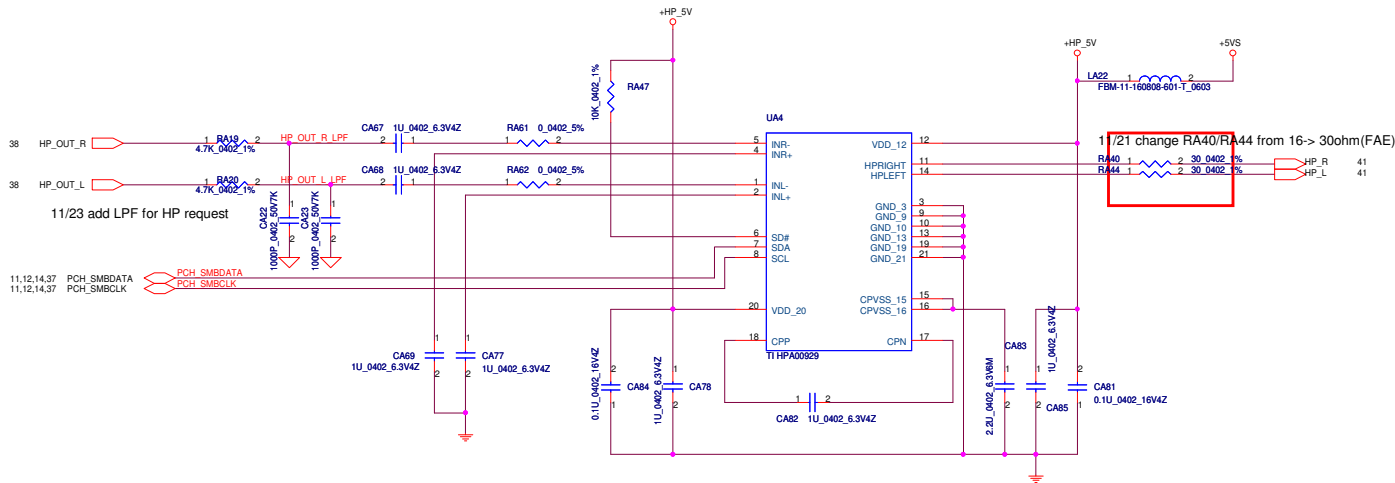
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/11/02	Deciphered Date	2011/11/02	Title	Audio IDT 92HD91
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				Date: Sunday, November 27, 2011	Sheet 38 of 57



2011.10.28 Change Sub-woofer Amp to TPA2011D1

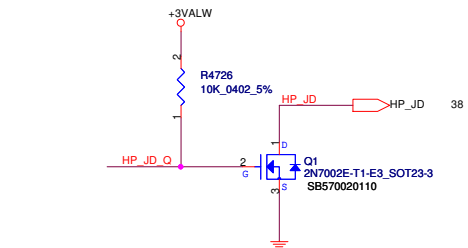
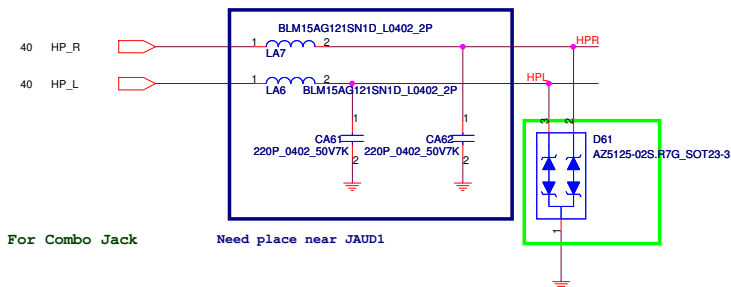
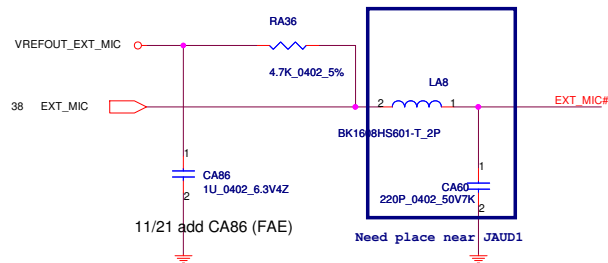
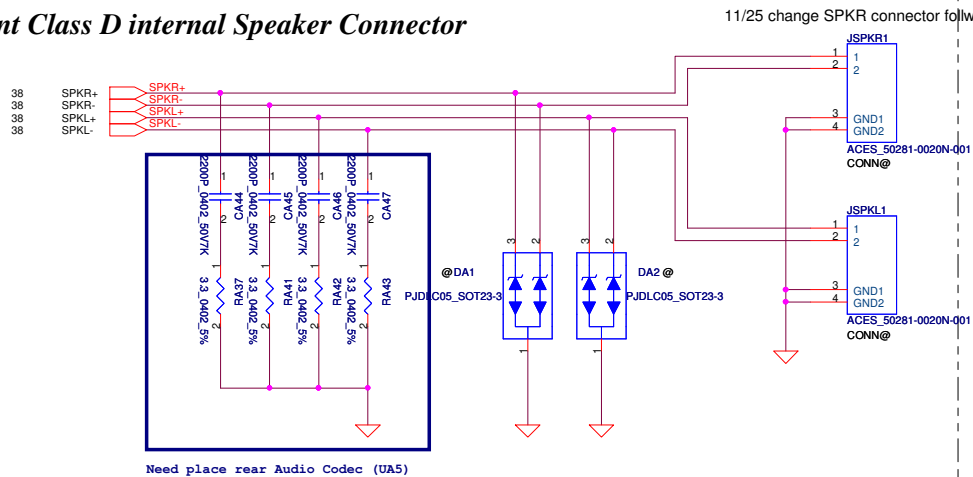
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Issued Date	2011/11/02	Deciphered Date	2011/11/02	Title	
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				Size B	Rev 0.1
Date: Sunday, November 27, 2011		Sheet 39 of 57			

Headphone Amp

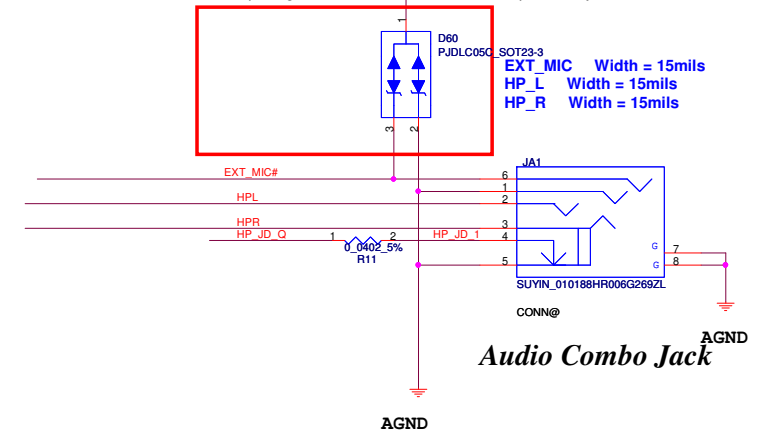


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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2011/11/02		2011/11/02		Audio SPK/HP Amplifier	
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Date:				Sunday, November 27, 2011	Sheet 40 of 57

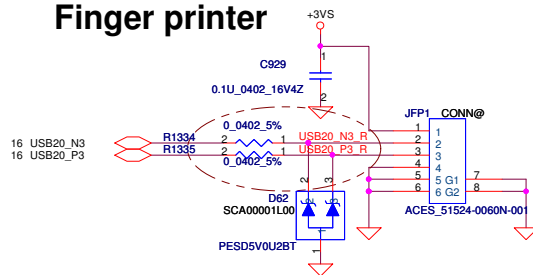
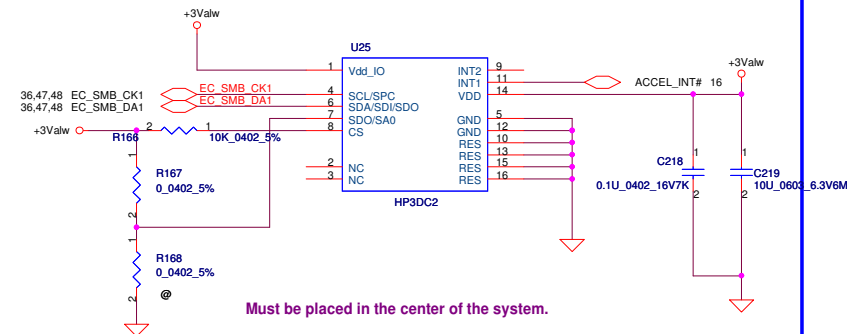
Front Class D internal Speaker Connector



11/23 spacing concern: remove DA4/DA5, keep D60 only



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				Date:	Sunday, November 27, 2011	Sheet 41 of 57



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				Document Number	0.1
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QC11 (LA-8551P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	mSATA MINI2	TP	SODIMM	EC_SMB_CK2 PCH_SMBDATA	PCH_SMBCLK PCH_SMBDATA	G-Sensor	GPU	AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V							V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					V
PCH_SMLCLK PCH_SMLDATA	PCH						V			V	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	USB3.0 FL1009-2Q0		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

: means Digital Ground



: means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI2
SATA1	m-SATA,JMINI1
SATA2	None
SATA3	None
SATA4	None
SATA5	None

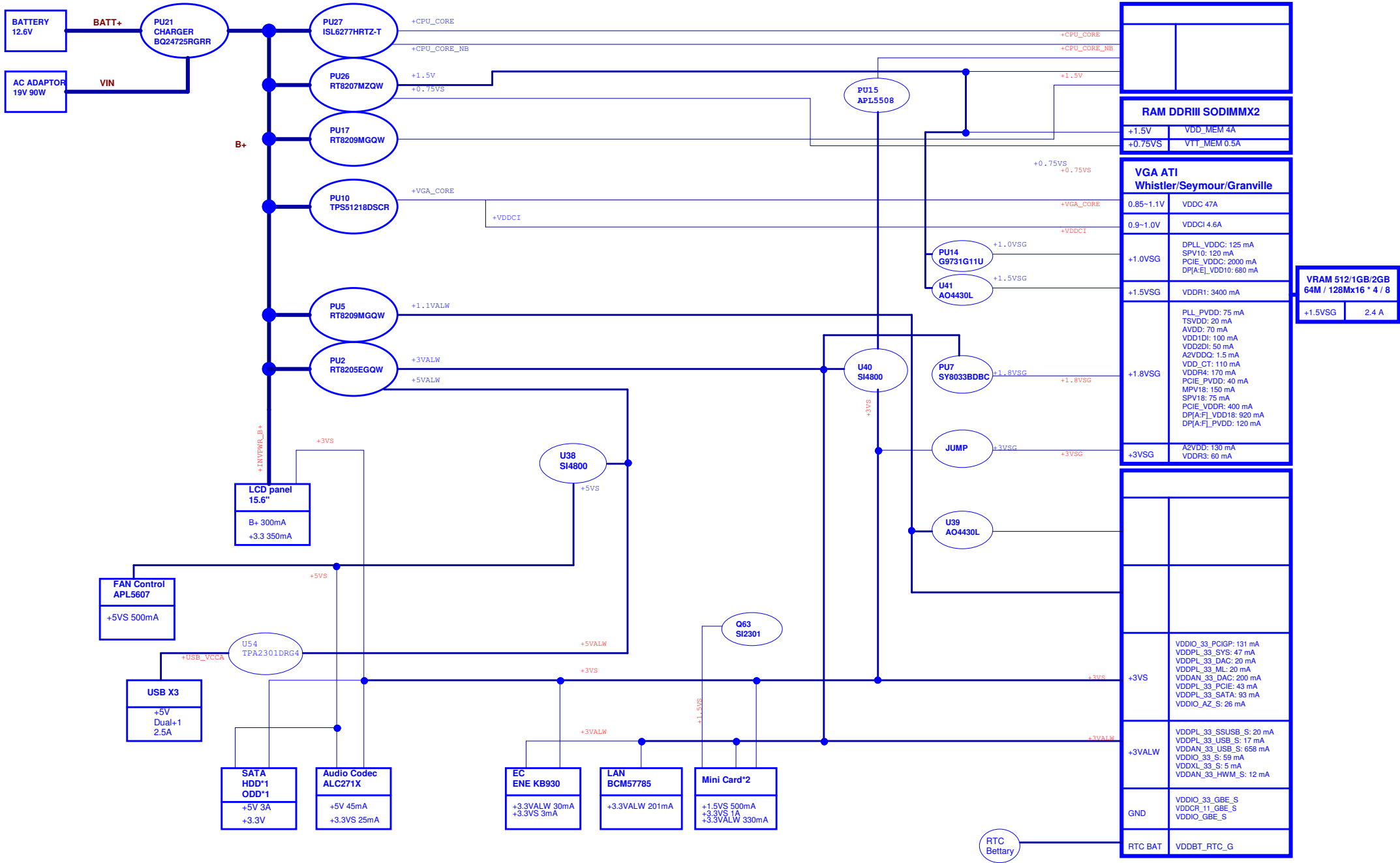
Option	@	CONN@	USB3.0@
UMA	X	X	V

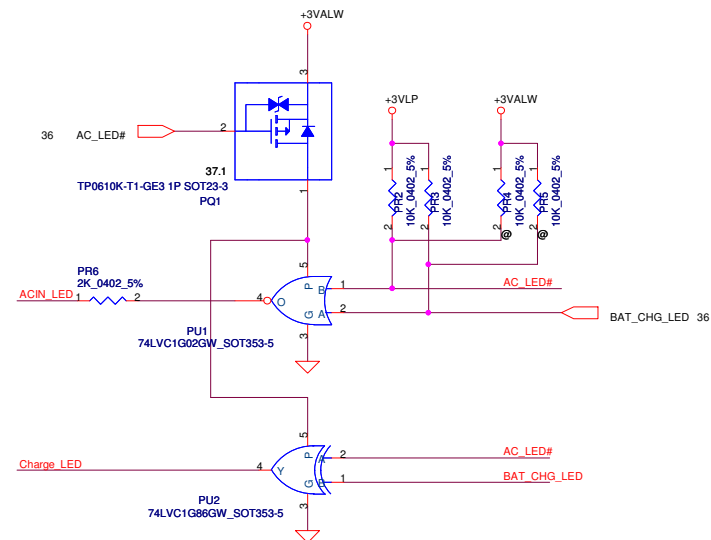
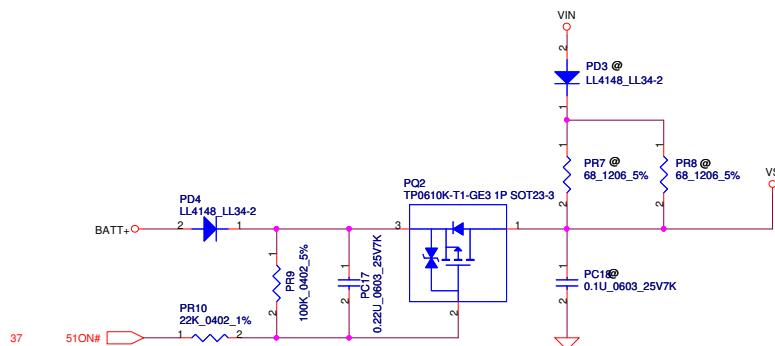
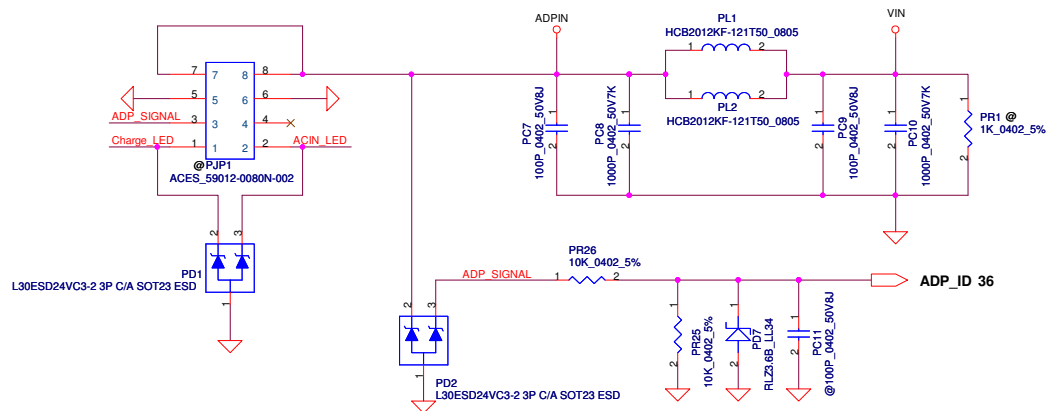
USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	m-SATA
EHCI2	UHCI3	6	
		7	
	UHCI4	8	Camera
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	

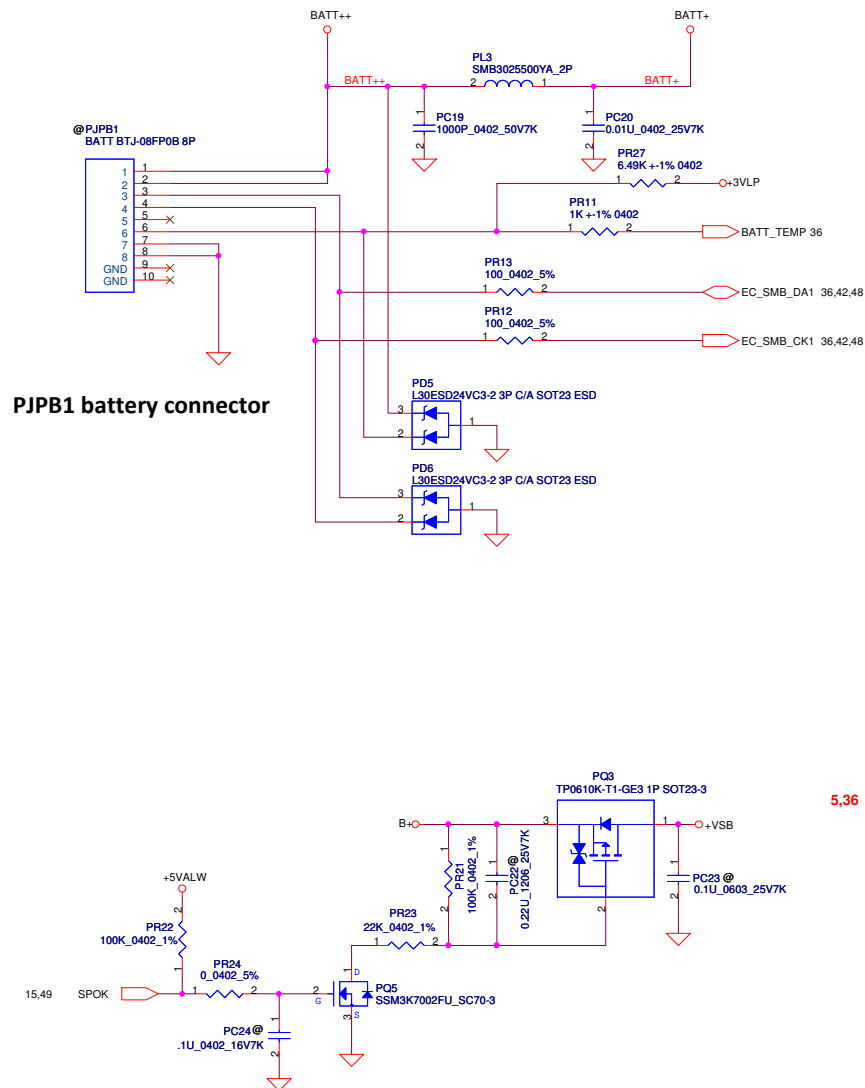
USB 3.0	Port	1 External USB Port
	0	
	1	

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									LA-8711	
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Deciphered Date				2014/12/31				PWR- DCIN / Vin Detector			
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				Rev				0.1			

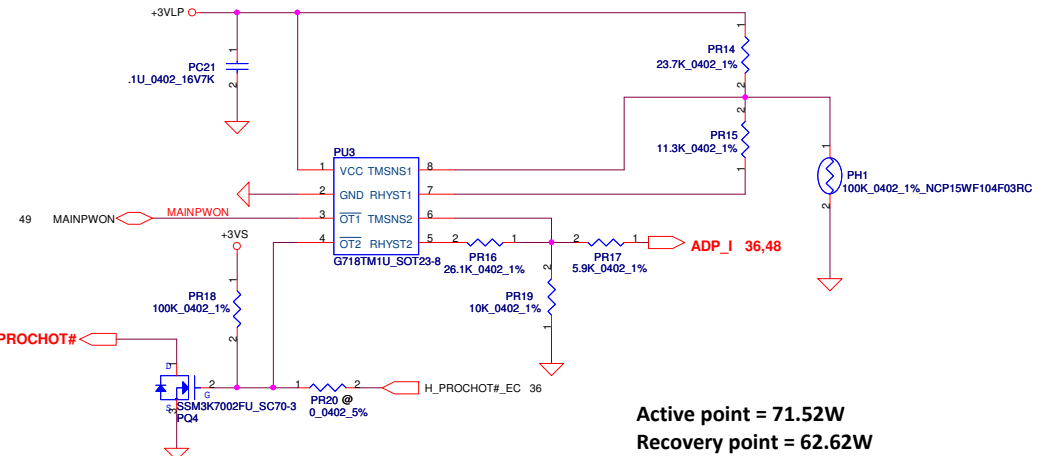


For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 --> Remove PU1 circuit, but keep PR25
PH1, PR15, PQ3, PR17, PR18, PR16
VCIN0_PH-->NTC_V
VCIN1_PH-->Turbo_V

PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
Recovery at 56 +/-3 degree C

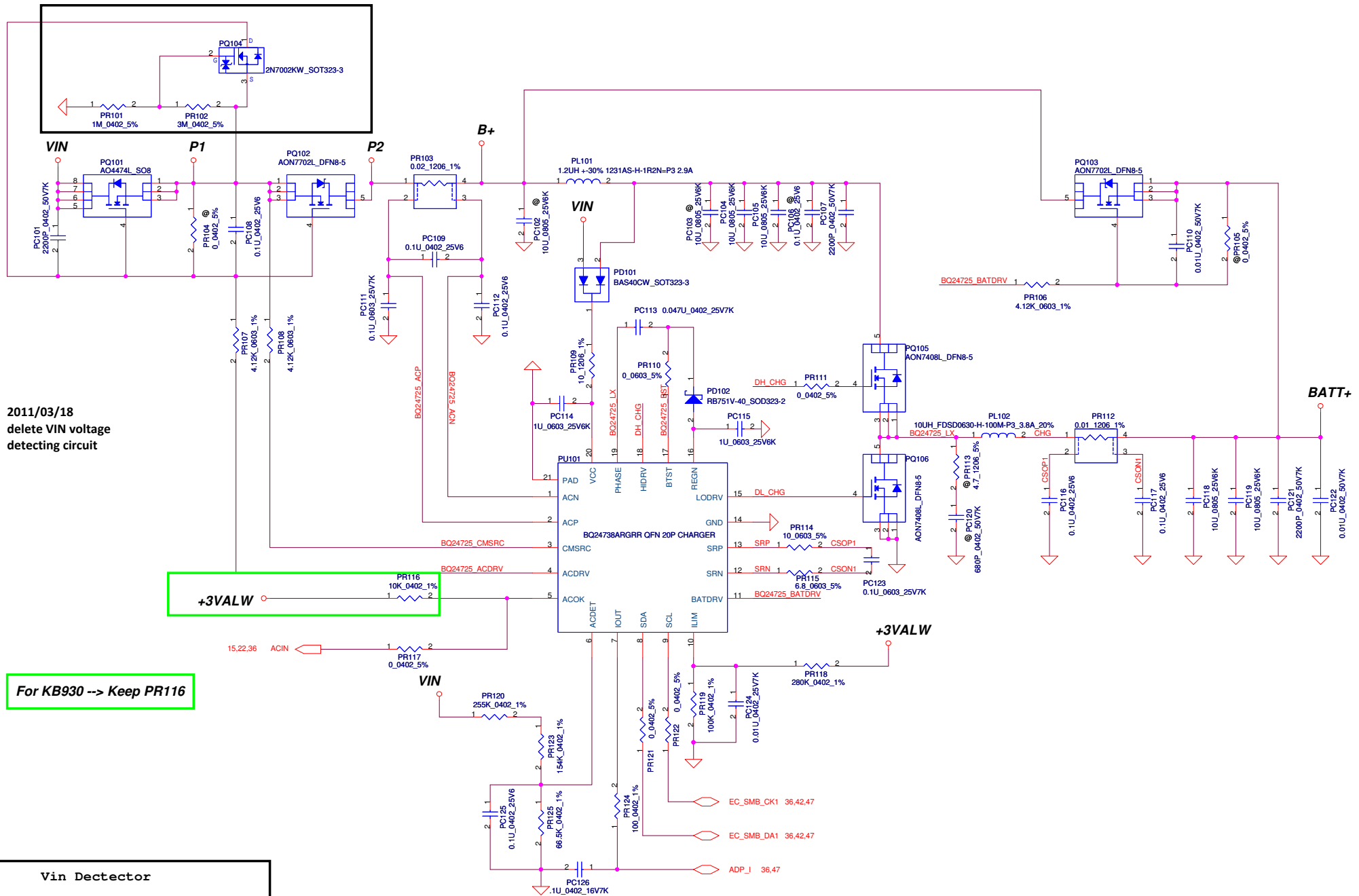
Rset = 3 * Rtmh
Rhyst = (Rset * Rtml) / (3 * Rtml - Rset)
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



Active point = 71.52W
Recovery point = 62.62W

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for reverse input protection



2011/03/18
delete VIN voltage
detecting circuit

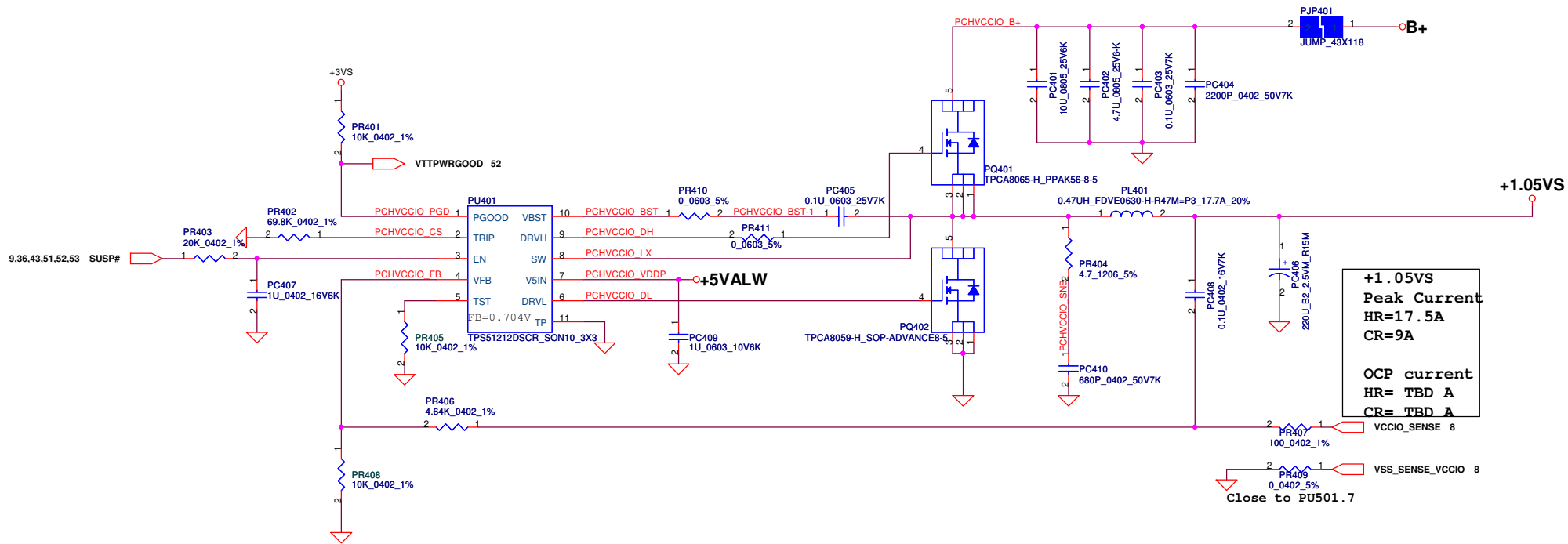
For KB930 --> Keep PR116

Vin Detector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

ILIM and external DPM
4.36A

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				Date:	Rev
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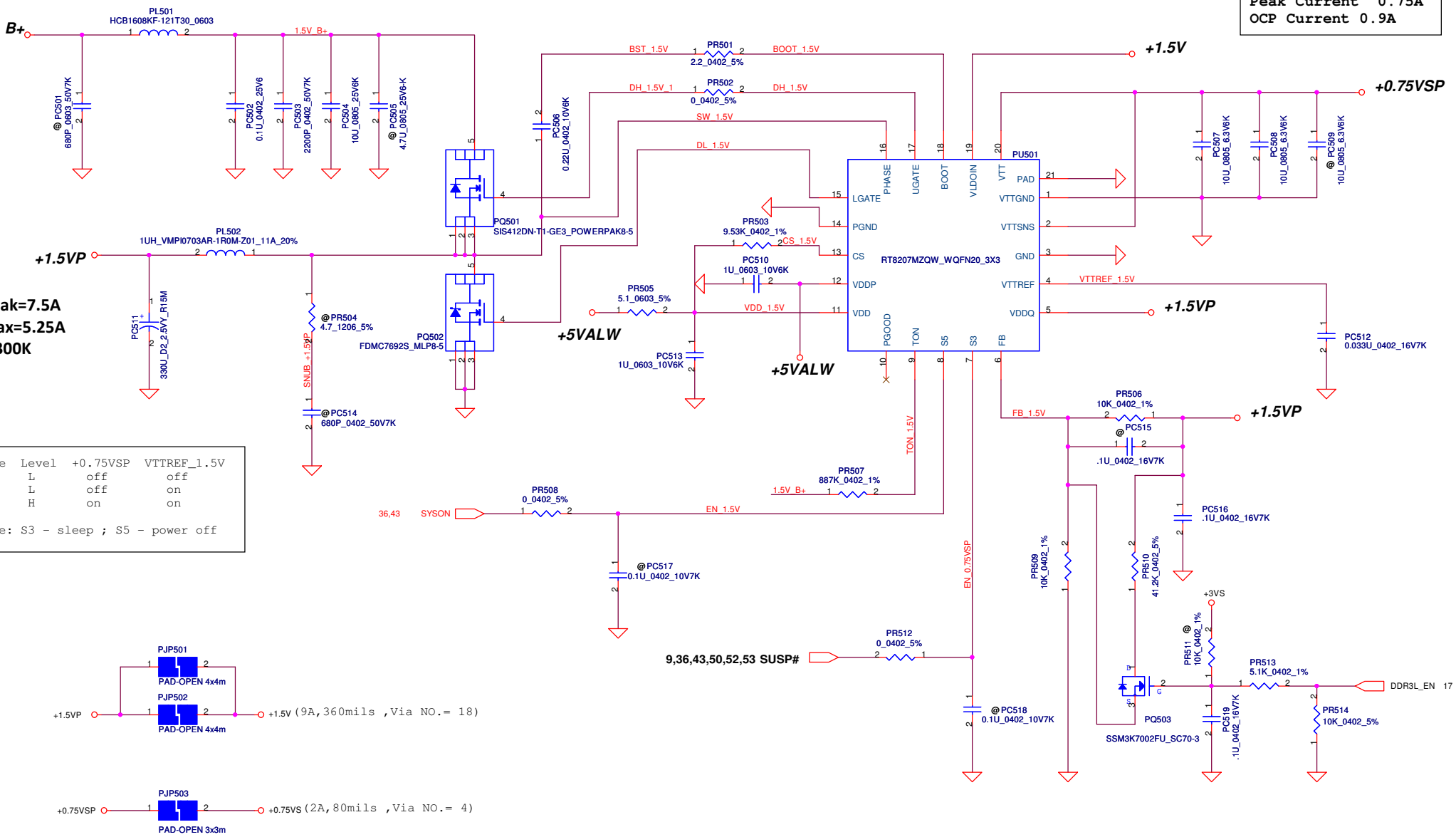
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Issued Date	2009/08/23	Deciphered Date	2011/12/31	Title	PWR-1.05VS
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I_{peak}=7.5A
I_{max}=5.25A
F=300K

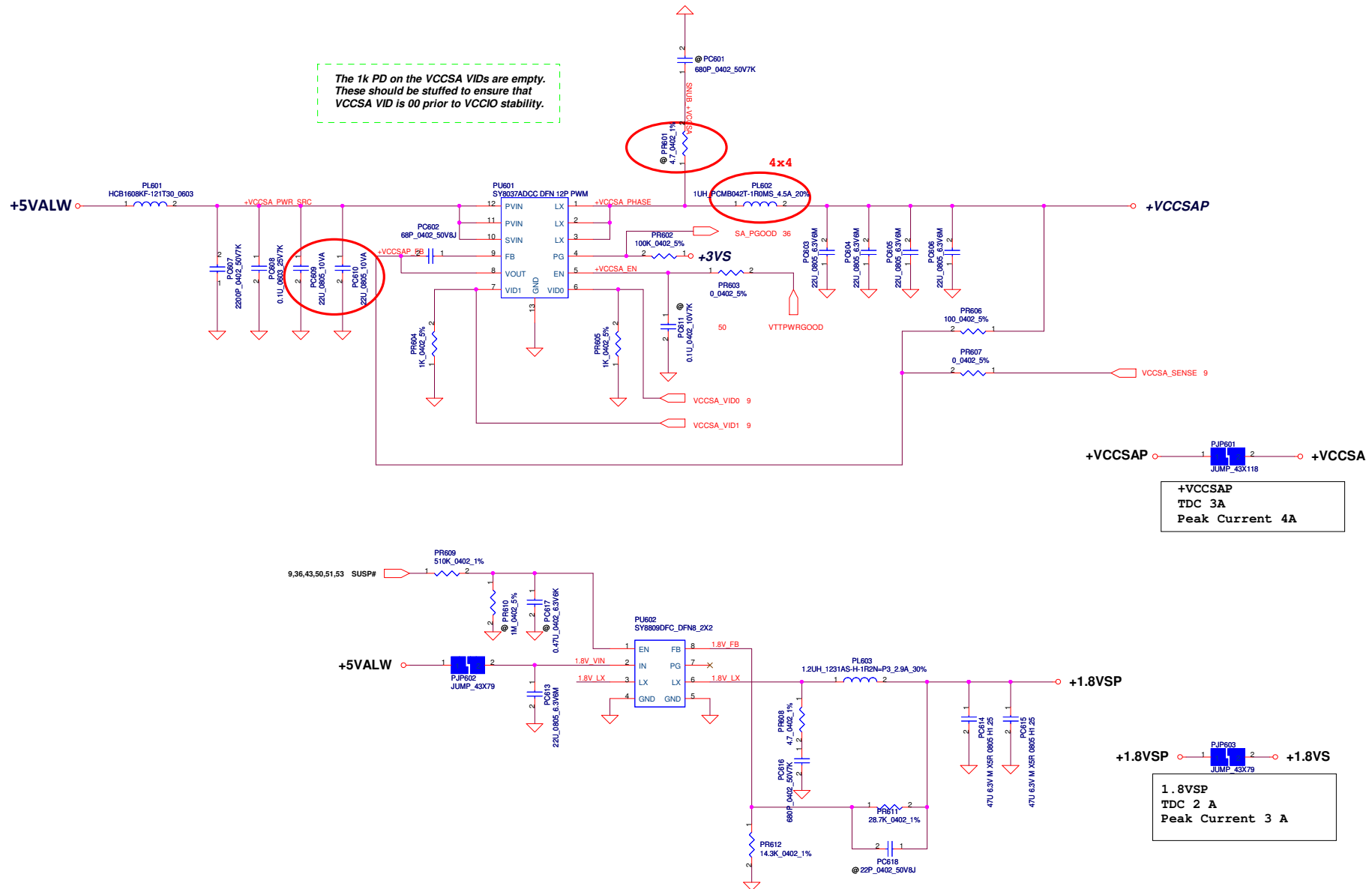
Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

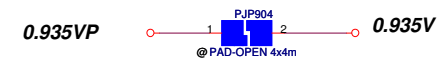
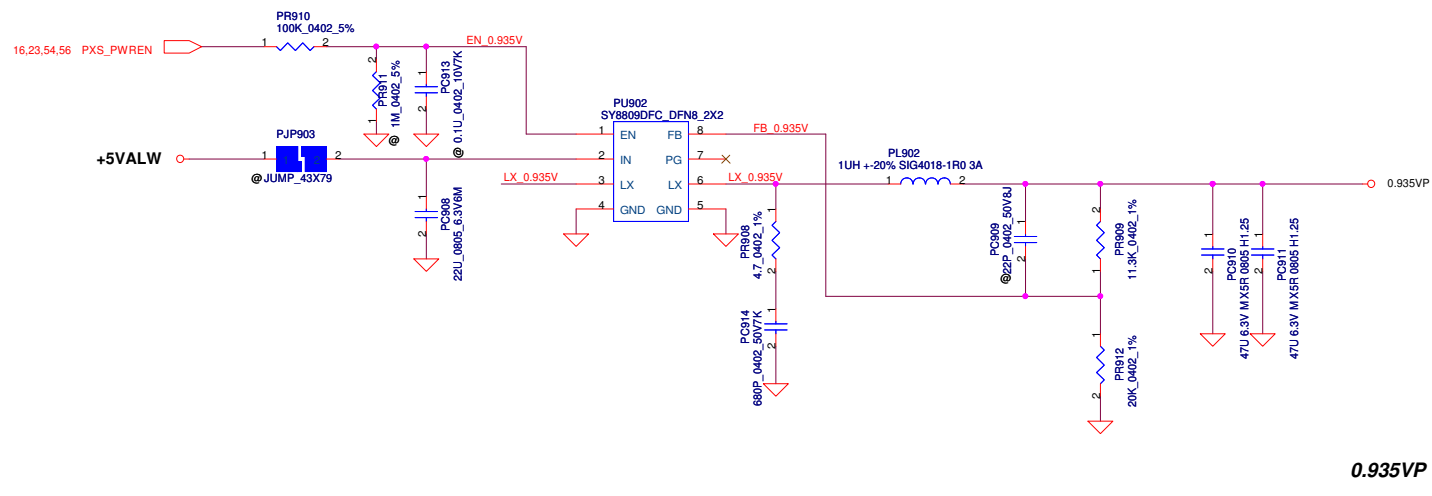
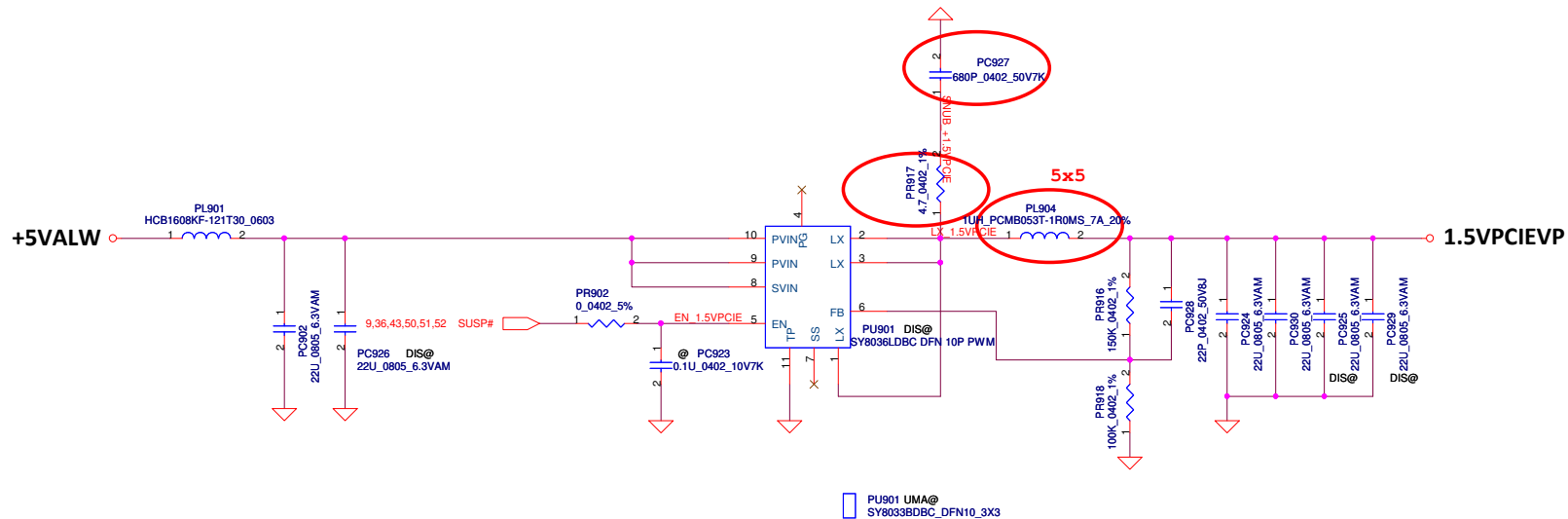
0.75V_{olt} +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



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Size	Document Number	Rev		0.01	
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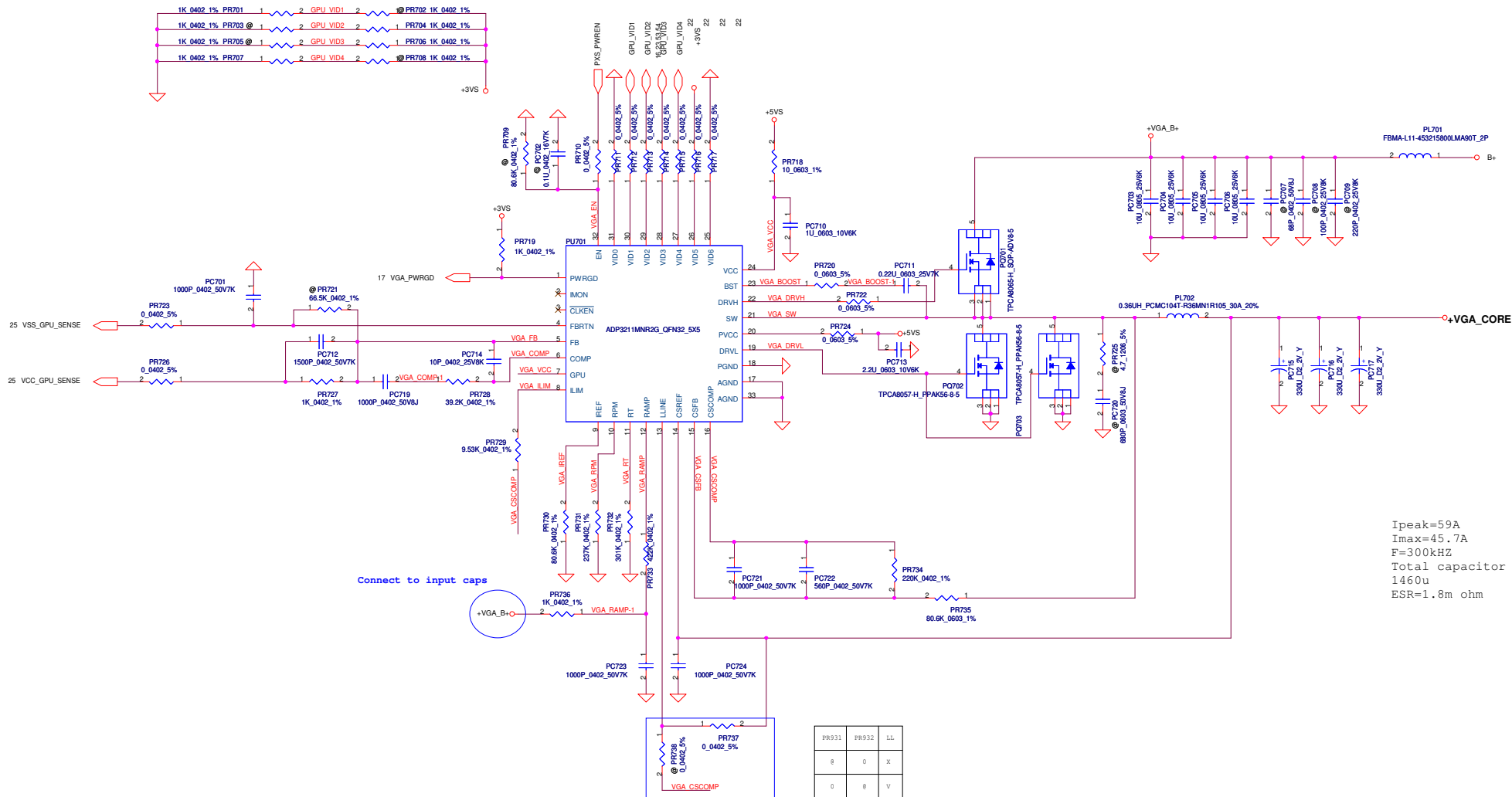
2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
 2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

2-ph: PR178=1.47K for -70A OCP

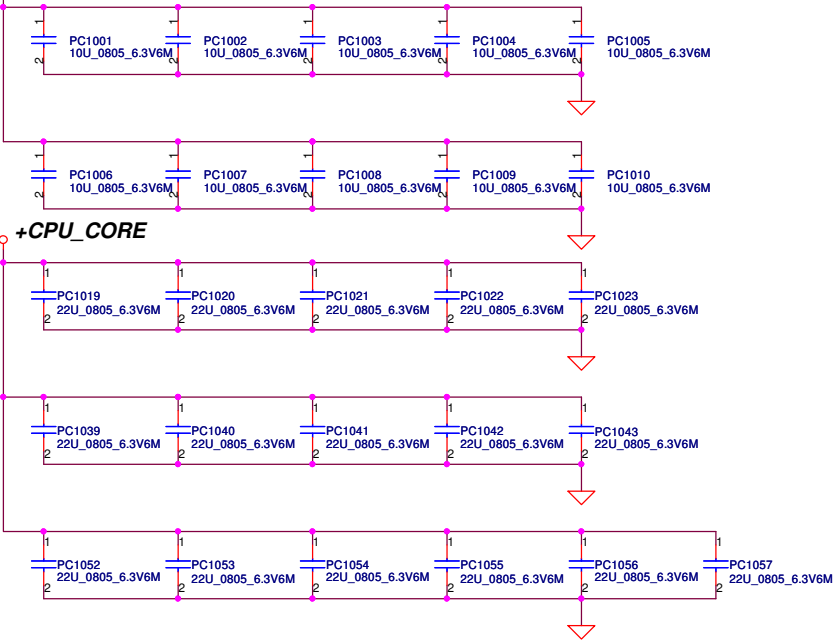
+CPU_CORE
 Iccp=72A, IccMAX=53A
 Load line=1.9mohm
 DCR=1.1mohm

+GFX_CORE
 Iccp=40A, IccMAX=24A
 Load line=3.9mohm
 DCR=1.1mohm

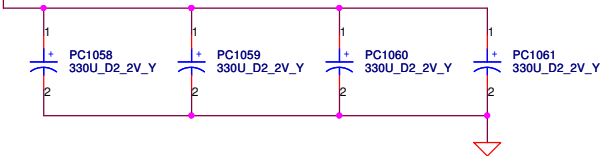
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2010/01/25		Deciphered Date		2009/04/28		Title					
								CPU_CORE/VGFX_CORE					
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						Date:		Sunday, November 27, 2011		Sheet		55 of 57	



+CPU_CORE

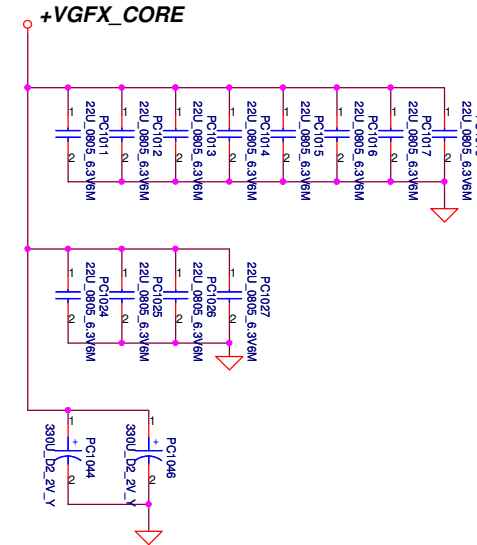


+CPU_CORE



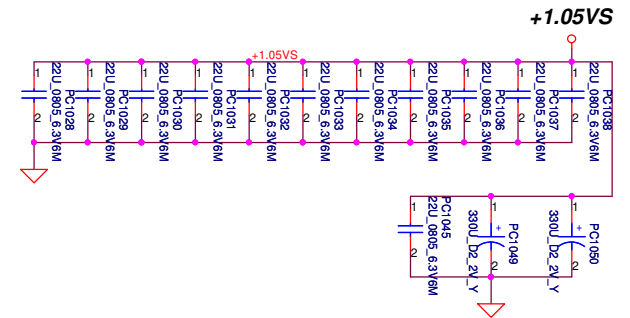
+CPU_CORE

+VGFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



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				Date	Sunday, November 27, 2011
				Sheet	57 of 57
				Rev	0.1